Analysis of VMM Operations on 1S1R Crossbar Arrays and the Influence of Wire Resistances

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***Abstract*—Memristive devices, such as ReRAM devices, enable Computation-In-Memory operations such as vector-matrix multiplications, which are basic kernels for neuromorphic computing. These devices, however, suffer from parasitic sneak path currents in memory arrays, which make a satisfactory performance on large-scale arrays impossible. To overcome this issue, for example, a bipolar rectifying element ('select device') in series to a resistive switching device (1S1R) is introduced at each cross-point junction. In this work, we investigate the design of 1S1R arrays for VMM operations and show the impact of wire resistances on these operations. We derive guidelines that give a quantitative relationship between the array size, wire resistance values, resistance states of the ReRAM and the select device and resulting current levels.**

Keywords—1S1R, crossbar array, VMM, wire resistance, select device, ReRAM cell, memristive device, read scheme, NDR

I. Introduction

Redox-based resistive memories (ReRAMs) are considered as a promising candidate for next generation nonvolatile storage solution [1-4] and for computation-in-memory (CIM) applications, e.g. neural network processes in hardware [5-7]. Corresponding emerging artificial intelligence (AI) technologies, such as deep learning, require highly efficient computation and are based on a huge number of "multiply-accumulate" (MAC) operations between input data and corresponding neural weights, in principle ordinary vector-matrix multiplication (VMM) operations [8,9]. Especially highly scalable $4F^2$ crossbar array architectures are investigated due to their feasibility to realize ultra-dense and energy-efficient memory device stacks [10,11]. The availability of a device that prevents parasitic currents in the array is a key enabler for large passive crossbar arrays, as these undesirable currents might occur during read/write operations affecting the current through unselected cells resulting in incorrect operations and degradation of the memory operation reliability [2,10-18]. An example for this kind of device is a volatile threshold switching select device in series to a memristive memory device (1S1R). Beside these 1S1R devices, the crossbar arrays consist of resistances of the wires that connect these and other devices in the crossbar array to each other [19,20].

In this work, we present studies on VMM operations on 1S1R crossbar arrays and additionally consider the general effect of linear wire resistances on the VMM operation, depending on the size of the crossbar array, on the resistance states of the devices and the resulting current levels.

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II. 1S1R Device Model

A. Model parameters

For the simulations, we use the JART VCM v1b model developed for HfO_2/TiO_x based ReRAM cell as presented in [21] for the nonvolatile memory device and the selector model proposed by Slesazeck et al. for a NbO_2-based threshold switch as volatile select device [22]. Here, we use the same parameter sets as in the referenced papers except for the changes stated below. The models are implemented using VerilogA, and SPECTRE, as implemented in CADENCE, is used for the circuit simulations.

Fig. 1 shows the simulated *I-V* characteristics obtained with these models using a sweep rate of 4 V/ms. In Fig. 1a, we observe a high resistive state (HRS) for the ReRAM cell, which turns into a low resistive state (LRS) after a SET event at a certain SET voltage. At some specific voltage in the reverse direction the RESET event occurs, and the memory device switches again into its HRS state. The state variable of the ReRAM device model, i.e. the physical variable defining the resistance state is the oxygen vacancy (defect) concentration in the so-called disc region N_{disc}, i. e. within the oxide region close to the active electrode. In the same way, the select device turns into its ON state at a certain threshold voltage after initially being in its OFF state. When the voltage now falls below a certain hold voltage, the device turns OFF again. This behavior is valid for both polarities. Therefore, it is a volatile device (Fig. 1b). The selector model's state variable is the temperature T_m.

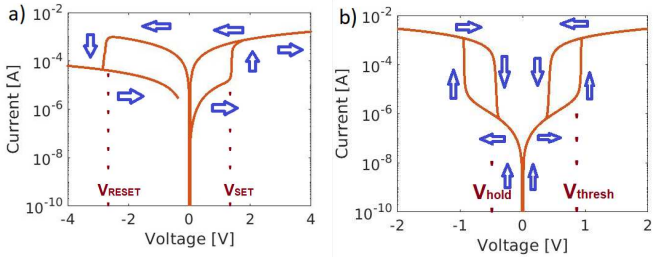

Fig. 1. Simulated *I-V* characteristic of a) the ReRAM cell; here, the switching polarity is defined in the opposite way compared to the JART VCM v1b model; and b) the select device.

The requirements that a select device and a ReRAM cell must fulfil for a combined 1S1R operation device are shown in Fig. 2. For the sake of simplicity, the required characteristics are illustrated with simple step functions, as these transitions occur abruptly, showing how the resistance states of the two devices depend on a positive voltage applied across the individual devices. At low bias the selector is in the OFF state and the ReRAM is in the HRS state. The OFF resistance of the select device has to be distinctly higher than the HRS resistance of the ReRAM cell, i.e. to control the current of the combined device and

consequently prevent high leakage current when the 1S1R device is not selected. The absolute value of the threshold voltage V_{thresh} for the select device must be modeled in a way that it is smaller than the SET voltage V_{SET} of the ReRAM cell. This requirement ensures that a read regime can be accessed while the select device has turned ON, but the ReRAM cell did not switch yet. The ReRAM resistance state can be now read without changing it. This also requires a select device hold voltage V_{hold} that is smaller than the voltage drop across the select device once it has turned ON. Otherwise, the select device will switch back to its OFF state and again switch ON etc. (voltage divider) affecting a system that will undergo switching oscillations. The read regime would not be accessible. The above-mentioned change of the voltage drop across the select device will occur due to its very low ON resistance state after turning ON and the voltage divider that is generated by the two devices being in series to each other. Once the SET voltage of the ReRAM cell is reached, the memory device switches to its LRS state and the write regime is entered. It is necessary that both resistance states of the ReRAM memory cell (LRS and HRS) are higher resistive than the ON resistance state of the select device, as once the 1S1R device has been selected for a read or write operation, it should be dominated by the ReRAM cell that is actually the crucial device for all operations performed on a crossbar array.

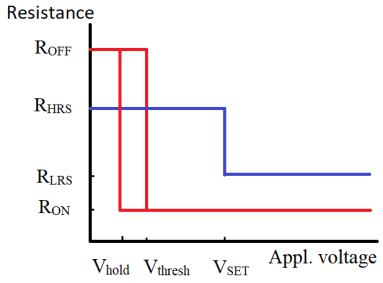

Fig. 2. Requirements to the resistance states, SET, threshold and hold voltages for a 1S1R device; the labels HRS and LRS refer to the ReRAM cell, ON and OFF are used in connection with the select device

In the following, some modeling parameters and their impact on the electrical characterization of the devices are described. For both devices, increasing the thermal conductance Γ_{th} will increase the absolute SET/threshold voltages for the *I-V* characteristic. (Note: In [21] the inverse of the thermal conductance is considered for the ReRAM cell: the thermal resistance $R_{th,eff}$.) Especially in the case of the select device, increasing the thermal capacitance C_{th} effects a widening of the hysteresis in the *I-V* characteristic: We observe the threshold at higher absolute voltages and a slight increase of the current in the ON state. Simultaneously, it leads to a smaller absolute hold voltage and to smaller currents in the OFF state. Changing one respective or both internal series resistances R_{series} of the respective models will lead to a change of the cell current. Tuning a combination of thermal conductance Γ_{th} (thermal resistance $R_{th,eff}$) and thermal capacitance C_{th} actually enables to achieve the requirement $V_{thresh} < V_{SET}$. When the combination of internal series resistances R_{series} and thermal capacitances C_{th} is tuned, we might get the relationship for the resistance states of the device: $R_{ON} < R_{LRS} < R_{HRS} < R_{OFF}$. A control of the leakage current or of the general current level can be achieved by a combined tuning of the series resistances R_{series} and the thermal capacitances C_{th}. Other selected crucial parameters regarding the *I-V* characteristic of the ReRAM cell are as follows: The initial (and minimum) oxygen vacancy concentration N_{init} (and $N_{disc,min}$), the maximum oxygen vacancy concentration $N_{disc,max}$, the nominal Schottky barrier $e\phi_{Bn0}$, the activation energy for ion hopping ΔW_A and the disc length l_{disc}.

All parameters mentioned above are adapted to fulfil the requirements for a 1S1R device as discussed before. To this end, the following parameters were changed while the remaining parameters are as in the original models [21,22]: $N_{disc,min}$ is set to $0.02 \cdot 10^{26}$ m^{-3}, $N_{disc,max}$ to $1.0 \cdot 10^{26}$ m^{-3}, $R_{th,eff}$ to $1.0 \cdot 10^{5}$ K/W for the ReRAM cell ($N_{init} = 0.02 \cdot 10^{26}$ m^{-3} for the HRS state; $N_{init} = 1.0 \cdot 10^{26}$ m^{-3} for the LRS state). In the selector model C_{th} is set to $2.5 \cdot 10^{-13}$ J/K, Γ_{th} to $1.0 \cdot 10^{-7}$ W/K, the resistance prefactor fitting constant R_0 is 340 Ω, the oxide thickness is set to 80 nm. The resulting resistance states and SET/threshold voltages for an applied rectangular voltage pulse are as follows: $R_{HRS} \approx 92$ KΩ, $R_{LRS} \approx 2.48$ KΩ, $V_{SET} \approx 1.3$ V voltage pulse for the ReRAM cell to experience a SET event within 200 µs pulse hold time (100 ps rise time), $R_{OFF} \approx 160$ KΩ, $R_{ON} \approx 832$ Ω, $V_{thresh} \approx 0.85$ V, $V_{hold} \approx 0.5$ V (select device).

B. Transient electrical characteristic

Fig. 3 shows the transient electrical characteristic for an applied rectangular pulse voltage of 1.5 V and 2.05 V to the 1S1R cell (HRS state), including the voltage that drops across the select device. The pulse rise time is chosen as 100 ps and the pulse hold time as 200 µs. For 1.5 V, a clear change in the voltage drop can be perceived, once the select device turns ON (Fig. 3a). Here, the applied voltage is sufficient and surpasses V_{thresh}. The current through the cell increases distinctly to a few microamperes. The voltage that drops across the ReRAM cell after the select device has turned ON, however, does not surpass V_{SET}. Therefore, this case displays the read regime. We again observe a fast voltage drop across the select device for 2.05 V, turning it ON (Fig. 3b). Also, a fast but slight current increase is visible after several microseconds. As now sufficient voltage ($> V_{SET}$) drops across the ReRAM cell after the selector has turned ON, we observe a SET event after a certain SET time of the memory device (≈ 100 µs). For higher voltage pulses, the SET time would be smaller, corresponding to the SET kinetics of ReRAM cells [23-26]. At the end of the voltage pulse, the current has increased to several hundred microamperes, as the LRS state is now obtained. One striking behavior is observed here: As an effect of the SET transition, one would expect that the voltage drop across the select device increases again (voltage divider). Here, a different scenario is perceived [22,27,28]: The voltage drop across the select device decreases further after the ReRAM cell has switched to its LRS state. This interesting observation can be explained by the the negative differential resistance (NDR) part in the selector's *I-V* characteristic with a series resistor. In the beginning, the voltage over the selector decreases, while the current futher increases, clearly showing the NDR of the selector device. As the ReRAM device is in the HRS state, the selector does not switch ON completely. For 2.05 V, the ReRAM device shows a SET transition. Thus, the select device can fully switch ON and a second NDR region appears (further voltage drop over the selector). Generally speaking, as the current through the select device increases, when being in series to another device, its voltage drop decreases. The select device, therefore, can only allow a higher current for a voltage

becoming smaller, its resistance decreases more than the resistance of the ReRAM device, when the latter device experiences a SET event to the LRS state. To capture this NDR effect, a physics-based or a mathematical model that describes the full dynamics correctly must be applied.

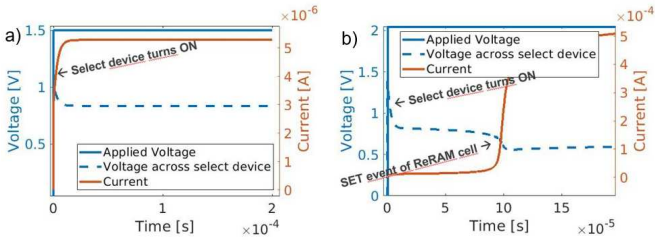

Fig. 3. Simulated transient electrical characteristics for an applied rectangular pulse voltage of a) 1.5 V and b) 2.05 V to the 1S1R cell (HRS state), including the voltage that drops across the select device and the resulting cell current

III. EFFECT OF WIRE RESISTANCES ON READ SCHEME

In this section, we discuss a 3x3 crossbar array, while we show the influence of wire resistances on the read scheme. In Fig. 4, the crossbar array consists of 9 1S1R cells and 18 wire resistances. The *V*/2 read scheme is used here. It states that the full read voltage will be applied on the selected cell by biasing the selected bitline (BL) and wordline (WL) accordingly. Half the read voltage is applied to all other so-called half-selected cells on the same BL and WL. All other BLs and WLs stay unselected and are not biased at all. We select the middle cell. Each cell will be read out after 50 µs.

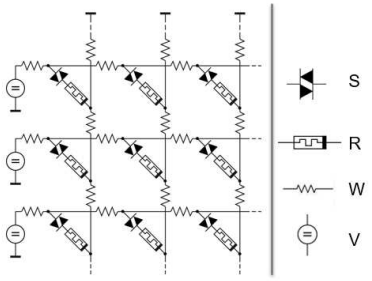

Fig. 4. 3x3 1S1R crossbar array with additional resistance wires before and after each cell, S represents the select device and R the ReRAM device, W denotes a wire resistance and V the voltage source

For the very first investigation, however, we exclude the select devices and all wire resistances. For case a) in Table I, we consider the worst-case configuration for the read scheme, e. g. the selected cell in the middle is in its HRS state, whereas all other cells are in their LRS state. We observe no current for the non-selected LRS devices, 118.6 µA each for the four half-selected LRS cells and 4.5 µA for the selected HRS cell. The total current on the selected BL amounts to 241.7 µA. This result shows that the read of the selected cell is not successful while not employing a select device. Introducing a select device improves the read-out operation distinctly. The cases b) and c) from Table I confirm this insight. In case b) we consider the same configuration as in a). The only difference is the inclusion of a select device connected to each ReRAM device (1S1R). The LRS half-selected cells read 1.01 µA each, the HRS selected cell in the middle reads 1.84 µA. In case c), all 1S1R cells are in the LRS state. The half-selected LRS cells again read 1.01 µA each, while the selected LRS cell in the middle reads a relatively high current of 197.1 µA. Despite the leakage current from the half-selected LRS cells (1.01 µA), the resistance state of the middle 1S1R cell can be read out reliably up to a crossbar array size of 194x194. Here, the maximum size was estimated by comparing the added up current of *x*-1 half-selected cells in LRS on the BL and of the full-selected HRS cell with the current of one LRS. This gives 1.84 µA + (*x*-1) · 1.01 µA = 197.1 µA and thus *x* = 194. This leakage current's degradation effect can be overcome with the use of an ADC through two well-defined current ranges (LRS vs. HRS) when reading a cell's state. A related issue will be discussed at the end of section IV. The cases d) and e) from Table I, for which the programmed device resistance states are similar to those in b) and c), respectively, show that introducing wire resistances (here: 1 kΩ each) into the crossbar array before and after each cell leads to a separation of the current levels. The four half-selected LRS cells will provide in total two different current levels due to an additional voltage drop across the wire resistances, instead of one single current level for all four cells. Furthermore, we measure a tiny reverse current through non-selected cells due to the same reason. These tiny currents will only have a very small impact on the read scheme. A similar approximation as before provides the insight that only a 60x60 crossbar array is feasible with the current levels that we get now (1.79 µA + (*x*-1) · 0.992 µA = 60.83 µA → *x* = 60). The values for this calculation are taken from Table I, d) & e). The presented calculation, however, only extrapolates the read currents from the 3x3 array to larger arrays without considering additional compulsory wire resistances for the additional wire connections as the array grows. Thus, the expected array size is even smaller.

TABLE I. READ SCHEME SCENARIOS

t_{read} = 50 µs V_{read} = 1 V (0.6 V for a)	Considered Cell in the 3x3 crossbar array			
	LRS, nonsel.	***LRS, half-sel.***	***HRS, selected***	***LRS, selected***
a) no wire res, only ReRAM	0 A	118.6 µA	4.51 µA	-
b) no wire res, 1S1R	0 A	1.01 µA	1.84 µA	-
c) no wire res, 1S1R	0 A	1.01 µA	-	197.1 µA
d) 1 KΩ wire res, 1S1R	-1.25 nA/ -2.53 nA	0.978 µA/ 0.992 µA	1.79 µA	-
e) 1 KΩ wire res, 1S1R	-0.99 nA/ -1.55 nA	0.612 µA/ 0.791 µA	-	60.83 µA

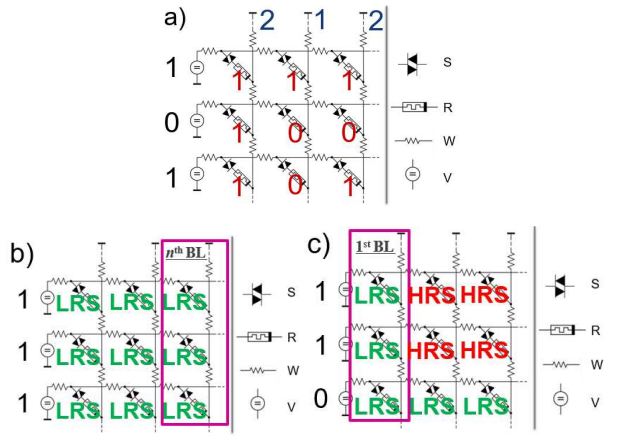

Fig. 5. a) VMM on a 3x3 1S1R crossbar array, b) array configuration for finding the lowest possible BL current with *n* LRS cells, c) array configuration for finding the highest possible BL current with *n* LRS cells

IV. EFFECT OF WIRE RESISTANCES ON VMM OPERATION

In this section, we first consider a 3x3 1S1R crossbar array to show some basic VMM behavior for single cells when wire resistances are introduced. Then, we move to bigger crossbar arrays up to 128x128 and determine which maximum wire resistance value is still feasible for a reliable VMM operation on a certain size of a crossbar array. Fig. 5a shows a common binary VMM operation on a 3x3 crossbar array. Here, the input voltage vector (1,0,1) is applied, 1 representing 1 V and 0 representing 0 V. The ReRAM devices are either in the LRS state (logical 1) or in the HRS state (logical 0) for $R_{ON} < R_{LRS} < R_{HRS}$. The *i*-th input voltage vector entry is multiplied with each of the ReRAM resistance state entries on the *i*-th crossbar row/WL for a certain column/BL of the array. All multiplication results on one BL are added up and give the resulting current for the BL. This is done for all columns/BLs whereas the input voltage vector is the same for each BL. Each resulting BL read current is one entry of the resulting current vector. In the same way, the VMM operation is performed for bigger arrays of any size.

When introducing wire resistances into the crossbar array for VMM operations, potential drops across these wire resistances will occur. Thus, every cell in the array experiences a different and individual added up wire resistance for the current that flows through it and its WL and BL. Therefore, the current levels through the cells differ from each other, although they have the same internal state and seem to be biased with the same voltage. The cell that sits in the farthest away corner from the WL voltage driver and the BL current read-out nodes experiences the highest amount of resistance wires on its current's path through the array. The cell that sits in the left-most top corner, i. e. the cell that is directly connected to the first WL voltage source and to the BL read-out node, only experiences the two wire resistances before and after it. Due to the resulting change of current levels for the individual cells, MAC and VMM operations might be highly disturbed. In the further work, we want the VMM operation to be reliable for the worst case, i.e. compare all cells on the farthest away (n^{th}) BL (lowest possible BL current) being in their respect. LRS state with all cells (one unbiased) being in their respect. LRS state on the nearest (1^{st}) BL (highest possible BL current). This is done by biasing all WLs in an array with 1, having all cells in the array in their respective LRS state, considering the n^{th} BL current level (shown in Fig. 5b exemplarily for a 3x3 array) and comparing it with another array that has all cells on its last n^{th} WL that is not biased in their respective LRS state; all other WLs are biased with 1, for these WLs all cells on the first BL are in their respective LRS state, whereas all other cells on these WLs are in their respective HRS state (shown in Fig. 5c exemplarily for a 3x3 array). Now the current level for the 1^{st} BL is considered and should be smaller than the n^{th} BL current of the previously considered array. Particularly the following practical rule must be fulfilled: $I_{nthBL}(n) \geq I_{1stBL}(n\text{-}1) + I_{1stBL}(n\text{-}1) / (2(n\text{-}1)) = I_{limit}$. Here the expressions *n* and *n-1* denote the number of cells in their LRS state on the corresponding BL, while *n*x*n* is the array size. I_{limit} is chosen as approx. $(n\text{-}1) \cdot I_{LRS}(1) \approx I_{limit}$, i.e. in a way that its exact value is approx. equal to (or possibly slightly bigger than) *n-1* times the current value of one single 1S1R LRS cell, i.e. $I_{LRS}(1) = 197.1\ \mu A$, as in bigger arrays the alternative limit $I_{1stBL}(n\text{-}1)$ is smaller due to potential drops. Another benefit is given by avoiding to choose $I_{1stBL}(n\text{-}1)$ as the upper edge current value, as $I_{1stBL}(n\text{-}1)$ can come very close to $I_{nthBL}(n)$ and a distinction between them might become difficult. We consider the results of this investigation done via circuit simulation which provide us with the largest admissible wire resistance for a successful VMM operation under a specific array size in Table II. The results generally display that as the number of wire resistances is scaled with the array size, it imposes limitations to a successful fully parallel VMM operation, depending on both, array size and wire resistance value. As we double the row and column number of the array, we simultaneously need to decrease the wire resistance value between half and one order of magnitude. This insight depicts a successful estimate of the relationship between array size and wire resistance value. Additionally, this estimate depends on the choice and tuning of the 1S1R device model parameters and the definition of the binary ReRAM resistance state (here: the value of N_{init}), resulting in well-defined current levels for a certain read-out time. Note that the investigation presented in Table II can be done at most for an array size *n*x*n*, while $I_{LRS}(1) > n \cdot I_{HRS}(1)$. In our case this will be a 107x107 array ($I_{HRS}(1) = 1.84\ \mu A$). For all bigger arrays an appropriate VMM operation is not possible anymore, as this condition now depicts the worst-case scenario. However, it is independent of the wire resistance, and rather depends on the select device's leakage current. When considering high wire resistance values, however, an effect of them will not stay negligible: A reduced current (by voltage drops on its connecting lines) of a biased farthest away cell in the LRS state (logical 1) shall not be smaller than the added up current of all biased HRS cells on the nearest BL experiencing almost no disturbance (logical 0).

TABLE II. VMM ANALYSIS

Array size, wire res value	**Current levels**				
	$I_{1stBL}(n\text{-}1)$	$I_{nthBL}(n)$		I_{limit}	*VMM possible?*
a) 8x8, 10 Ω	1.27 mA	1.25 mA		-	**No**
b) 8x8, 5 Ω	1.32 mA	1.40 mA	<	1.42 mA	**No**
c) 8x8, 4 Ω	1.33 mA	1.43 mA	=	1.43 mA	**Yes**
d) 16x16, 1 Ω	2.86 mA	2.88 mA	<	2.95 mA	**No**
e) 16x16, 0.5 Ω	2.91 mA	3.01 mA	>	3.00 mA	**Yes**
f) 32x32, 0.1 Ω	5.98 mA	6.10 mA	>	6.07 mA	**Yes**
g) 64x64, 0.05 Ω	12.03 mA	11.84 mA		-	**No**
h) 64x64, 0.01 Ω	12.30 mA	12.45 mA	>	12.40 mA	**Yes**

V. CONCLUSION

A threshold select device in series to the memory device leads to a distinct improvement of read and VMM operations. Wire resistances in a 1S1R crossbar array strongly limit the array size for a successful VMM operation, affected by the interplay of array size, wire resistances, device resistance states and current levels. Possible mitigation options as limiting parallelism by (1) only biasing part of the WLs at a time and/or (2) measuring on part of the columns and biasing the others at some voltage need to be considered in future. Another observation made is that when turning the select device ON and/or setting the memory device (1S1R), an NDR for the former device can be observed in the electrical characteristics. This leads to a decrease of the voltage drop across the select device while the current through it is increasing. In this atypical voltage divider consideration, the resistance of the select device decreases more than the memory cell resistance, when the latter cell sets and the select device is in its ON state before.

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