Experimental and Theoretical Analysis of Stateful Logic in Passive and Active Crossbar Arrays for Computation-in-Memory

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***Abstract*— As the cost of keeping Moore's law alive is ever increasing, unconventional device and circuit concepts are being explored, both in industry and in academic research arena. Among the new devices being explored are two terminals redox-based memristive devices, which can function as both a nonvolatile memory and a computing element. For enabling Computation-in-Memory (CIM) concepts, these devices are generally integrated in a passive configuration or in an active configuration, where transistors are employed together with the memristive switches. However, the reliability and variability of the memristive devices might impact the performance of CIM circuits. In this work, we experimentally demonstrate the impact of device-to-device (D2D) and cycle-to-cycle (C2C) variability on a simple IMPLY logic gate realized in passive and active configurations. The experimental data is theoretically verified by a physics based Verilog-A model of the memristive devices. Our findings suggest that the success rate of the logic operation can be increased by exploiting the D2D variability in the memristive devices.**

I. Introduction

Redox-based resistive devices (ReRAM devices) based on the Valence-Change-Mechanism (VCM devices) are considered as future storage class memory elements [1] [2, 3] or as fundamental building blocks for CIM [4-10]. By applying voltage pulses of different polarities their resistance can be decreased (SET process) or increased (RESET process), which means the devices are bipolar [11]. As only a small portion of the total device area is involved in the switching process the switching can be characterized as filamentary [12].

Widespread commercialization, however, remains difficult due to their substantial variability. Additionally, different applications have different requirements regarding the toleration and types of variability. Stateful logic concepts such as MAGIC [9, 13], or IMPLY [14, 15], that require initialization of the devices as well as writing of the devices to perform a logic operation have for example higher reliability requirements than logic concepts such as Scouting logic [16, 17], which only requires an initial programming and then uses read operations together with different periphery configurations to perform the logic functions. The advantage of the stateful logic concepts is that the outcome of the logic operation is directly stored in the memory element, showing a true computation-in-memory (CIM) concept. Since their requirements with regard to variability and device non-idealities are more stringent, a close connection during the design of stateful logic gates between the experimental and the simulation level is required. While experimental realizations are seen to be the most valid kind of results, in the earlier stages of the design process they are not necessarily available. Furthermore, it is usually easier to generate larger statistics and to investigate larger circuits in more details [16][8, 18].

To perform valid and useful simulations, predictive circuit level models are required. The relevant types of variability, be it device-to-device (D2D) or cycle-to-cycle (C2C) have to be experimentally quantified and then described using these models before any circuits are investigated [19, 20]. In this work, we present experimental and simulative investigations of the stateful IMPLY logic gate [14]. We consider two different filamentary bipolar VCM devices, namely ZrO_2 and TaO_x, describing them through experiment and simulation. The ZrO_2 devices are thereby investigated in a passive 32 x 1 line array structure, whereas the TaO_x devices were co integrated together with a custom transistor technology (1T-nR line arrays), enabling the investigation of the possibility of replacing the series resistor by a series transistor in an active configuration.

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II. Fabrication and Simulation Model

A. Fabrication

For the investigation of the passive configuration 10 µm x 10 µm crossbar devices are fabricated with a 30 nm Pt/5 nm ZrO_2/20 nm Ta/30 nm Pt stack. Reactive radiofrequency (RF) sputtering is employed to deposit ZrO_2 on the Pt bottom electrode (BE). The Ta top electrode (TE) is added after a lithography step via RF sputtering and *in situ* covered by 30 nm Pt to prevent oxidation. The crossbar devices are arranged in groups of 32 devices that share the BE.

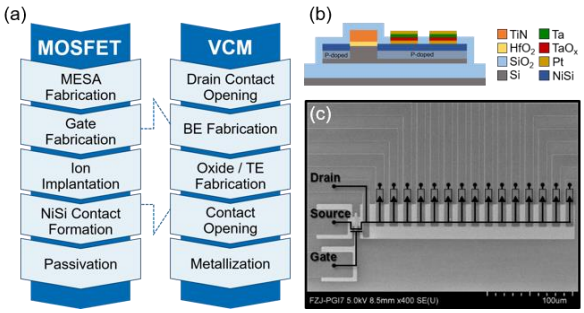


Fig. 1: (a) Process flow of SOI MOSFET and RRAM fabrication. (b) Schematic diagram of the 1T-2R device structure. (c) SEM image of the resulting 1T-nR structure, schematically showing the location of the transistor and TaO_x RRAM devices.

The active configuration (1T-nR) consists of a transistor and multiple TaO_x VCM devices, integrated directly on drain region. For the MOSFET fabrication, a gate-first process with self-aligned NiSi S/D contact is developed on 30-nm-thick Silicon-on-Insulator (SOI) substrate. The 2 µm channel length was patterned with 5-nm-thick ALD deposited HfO_2 and 40-nm-thick sputtered TiN as gate stack. Subsequently, a 2 µm x 2 µm Pt/10 nm TaO_x/15 nm Ta/Pt device is integrated on the drain region. As final step, 300-nm-thick Al is used to form the contact pads for the MOSFET and VCM devices. The process flow, layout and illustrative cross-section are shown in Fig. 1.

B. Simulation Model

The simulations were performed using the physics-based compact model JART VCM v1b var [21] which has been shown to be able to reproduce the variability of filamentary and bipolar VCM devices for various experiments such as *I-V* sweeps, SET and RESET kinetics, endurance experiments [22] and also stochastic SET experiments [23]. The model parameters are fitted to describe the measured experimental data in Fig. 4 (a). The resulting parameter set can be seen in Table I.

For an explanation of the meaning behind the parameters we refer the readers to [22, 23]. As the transistors were fabricated in a custom process, we adapted a 130 nm PTM model to describe the output characteristics over the relevant range of Gate-Source voltages, shown in Fig. 2 (a) and (b).

C. IMPLY in passive and active configurations

Among the most investigated concepts for CIM concepts is the so called IMPLY logic concept [14-15, 24-25]. The usual circuit to perform this logic function using two VCM devices and one series resistor is shown in Fig. 3 (a). Alternatively, it is possible to replace the series resistance by a transistor biased via a constant gate voltage, cf. Fig. 3 (b). Fig. 3 (c) shows the corresponding truth table for the four possible combinations of *p* and *q*. As the IMPLY logic requires a SET operation of one of the devices it can be classified as a SET logic in contrast to the RESET logic types [26].

TABLE I: Simulation Parameters

$A_{det} = \pi\, r_{det}^2 = 2.83^{-15}\ m^2$	$r_{det} = 30$ nm
$N_{disc,\ min,\ det} = 0.002*10^{26}\ m^{-3}$	$N_{disc,\ max,\ det} = 1*10^{26}\ m^{-3}$
$N_{disc,\ init,} = 0.38*10^{26}\ m^{-3}$	$N_{plug} = 20*10^{26}\ m^{-3}$
$l_{cell} = 5$ nm	$l_{det} = 0.4$ nm
$l_{plug} = 4.6$ nm	$R_{th,\ line} = 90471.47$ K/W
$R_{series} = 100\ \Omega$	$\Delta W_A = 1.6$ eV
$a = 0.25$ nm	$\alpha_{line} = 3.92*10^{-3}$ 1/K
$\nu_0 = 5*10^{12}$ Hz	$\mu_n = 4*10^{-6}\ m^2/(Vs)$
$R_{th0,\ SET} = 15*10^6$ K/W	$R_{th0,\ RESET} = 7.5*10^6$ K/W
$e\Phi_{Bn0} = 0.18$ eV	$e\Phi_n = 0.1$ eV
e=1.6*10^{-19} C	$m^* = 9.11*10^{-31}$ kg
$A^* = 6.01*10^5\ A/(m^2K^2)$	$T_0 = 293$ K
$k_B = 1.38*10^{-23}$ J/K	$z_{vo} = 2$
$\varepsilon_{\Phi B} = 5.5*\ \varepsilon_0$	$\varepsilon_0 = 8.854*10^{-12}$ As/(Vm)
$h = 6.626*10^{-34}$ Js	$\varepsilon = 17*\ \varepsilon_0$
$W_{Transistor} = 2.2$ µm	$L_{Transistor} = 2$ µm
Variability parameters	
Symbol	**Minimum/Median/Maximum**
$N_{disc,\ min,\ var}\ [10^{26}/m^3]$	0.001/0.002/0.003
$N_{disc,\ init,\ var}\ [10^{26}/m^3]$	37/38/39
$N_{disc,\ max,\ var}\ [10^{26}/m^3]$	0.5/1/20
r_{var} [nm]	25/30/35
l_{var} [nm]	0.25/0.4/0.6
	Value
relative standard deviation	1
c2c percentage	15 %
maximum step size	10 %

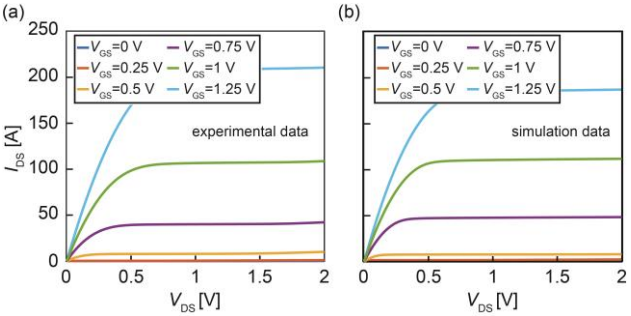
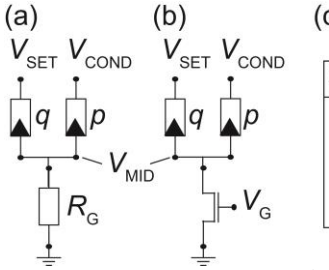


Fig. 2: Experimental (a) and simulated (b) output characteristics of the fabricated and simulated MOSFET for various V_{GS} voltages (0 -1.25V).



Case	p	q	q'
1	1	1	1
2	1	0	0
3	0	1	1
4	0	0	1

Fig. 3: Schematic circuit diagrams of the passive (a) and active configuration, which were used to investigate the IMPLY logic function. The truth table of the IMPLY logic is shown in (c).

III. Passive Crossbar Array

For showing the feasibility of our proposed concepts, we investigated different material systems. For the passive configuration ZrO_2 devices were measured. As the IMPLY logic requires finding two voltages namely V_{COND} and V_{SET}, that are supposed to allow or prevent a SET process depending on the voltage divider configuration between the

two VCM cells and a series resistance, the variability of the SET process is of special interest for this type of logic. To study the D2D and C2C variability, the SET probability as a function of the applied SET voltage is measured for 5 different devices. The results are shown in Fig.4 (a) with the corresponding simulations shown in Fig.4 (b). For experiment and simulation, the devices are initialized in the HRS between 20 kΩ -50 kΩ and SET voltages between 0.5 V and 1.5 V were applied for 100 µs. At each voltage the experiment was repeated for 200 times to achieve a reliable statistic. The resulting current before and after the application of the SET pulse was measured at V_{READ} = 200 mV. If the resulting resistance is found to fall below 12 kΩ the SET was interpreted as successful. As expected for these types of devices [23] the behavior can be split into three parts. At low voltages the cells show deterministic non-switching behavior, at medium voltages they show stochastic switching and at high voltages they show deterministic switching. The stochastic switching is a consequence of the C2C variability. However, it can clearly be observed that these regions vary for different devices, highlighting the D2D variability. This experiment can be seen as a case study to distinguish the D2D and C2C variability. Combined with the IMPLY logic, it supports the need that these two kinds of variability need to be evaluated in their impact separately. Assuming a single SET probability curve as shown by the red thicker curves in Fig. 4 (a), (b) ignores the differences among different devices. Furthermore, these results suggest that the success rate of the logic will strongly depend on the assignment of

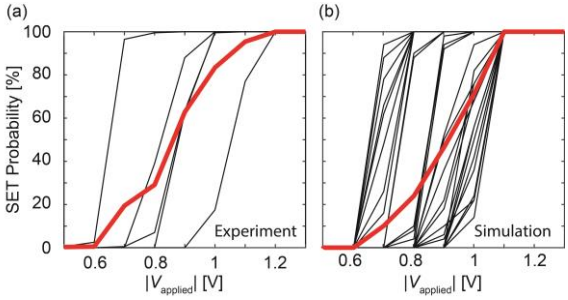


Fig. 4: Experimental (a) and simulated (b) SET probabilities as a function of the applied voltage for a 100 µs pulse. The black curves in both cases show the SET probabilities of individual devices, while the thick red curve shows the mean SET probability curve.

cells to the input variables p and q for the selected cells. As the SET probability curve cannot be chosen for a device, the experiments are performed with arbitrary assignment of p and q. The resulting success rates can be seen in Fig. 5 (a) for case one (p/q=1/1), Fig. 5 (b) for case two (p/q=1/0), Fig. 5 (c) for case three (p/q=0/1) and Fig. 5 (d) for case four (p/q=0/0). In all the experiments the series resistance was chosen as 18 kΩ. For cases 1 and 3, nine arbitrary combinations of p and q cells were measured ten times at every SET voltage. The V_{SET}/V_{COND} ratio was kept constant at 0.5 and the success rates were averaged over all combinations. The LRS was kept between 1-15 kΩ and the HRS between 90-140 kΩ. As is to be expected, cases one and three can easily achieve very high success rates > 95 %, while cases two and four are more difficult. For the investigation of cases two and four, we performed a thorough study of the influence of the SET voltage and V_{SET}/V_{COND} ratio. For these investigations the LRS was chosen between 0.5-4 kΩ as the smaller range improves the stability of q in case two, whereas the HRS was kept between 90-140 kΩ. At each combination of V_{SET} and V_{SET}/V_{COND}, 10 measurements were performed in 12 different, arbitrary device combinations, with the success rate depicting the average of all results.

In case 2, (p/q=1/0) the possible error is the switching of q. This explains the better performance of case two at smaller SET voltages and higher V_{SET}/V_{COND}, where 100% success rates are possible. Although the switching of p would technically not be the wrong end result, as only the future state of q (q') determines the success of the logic operation, a switching of p would mean that the devices would have to be initialized after each logic operation, greatly decreasing the energy-efficiency and operation time. For case 4, the best results are observed at large V_{SET} and small V_{SET}/V_{COND} ratios since in this region it is most likely that q will switch. These results, however, show the problem with this type of logic, namely that for different input cases, the optima can differ or lie in opposite directions. The optimum combination of the

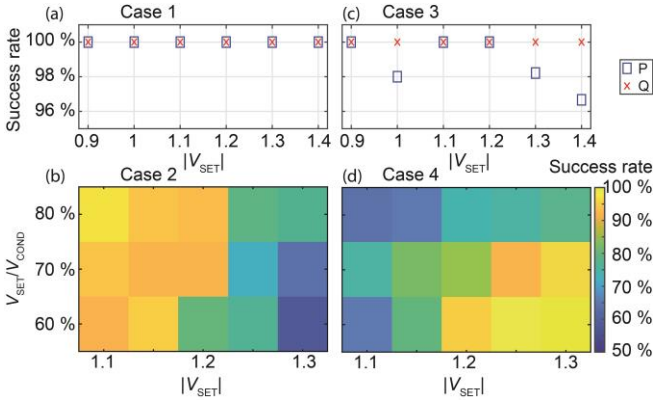


Fig. 5: Experimental success rates of the IMPLY operation split up into the different input combinations. (a) shows case one (p/q=1/1), (b) case two (p/q=1/0), (c) case three (p/q=0/1) and (d) case four (p/q=0/0).

V_{SET} and the V_{SET}/V_{COND} lies at 1.2 V and 0.7 V respectively, giving an overall success rate of 78%.

IV. Active Crossbar (1T-nR) Array

The possibility to co-integrate transistors as an active component with VCM cells enables the investigation of their interplay on logic operation. As the output characteristic of the transistor shown in Fig. 2 (a) demonstrates, the gate-source voltage V_{GS} defines the channel resistance in the linear region and the load current in saturation region. In the linear region, the transistor works as a series resistor connected to the TaO_x VCM cell and leading to a voltage divider during SET and RESET operations. In the saturation region, the transistor limits the load current, which consequently applies an intrinsic current compliance to the TaO_x VCM cell in series during its SET operation and thus defines the Low Resistive State (LRS). In addition, this minimizes the overshoot current which has been shown to be able to destroy devices [27, 28]. Upon introduction of the transistor, the active configuration requires an additional V_{GS} in addition to V_{SET} and V_{COND} in order to operate the logic function. Because the V_{GS} simultaneously determines the series resistance of the transistor and the LRS of the VCM cell, which both affect the functionality of stateful logic, it becomes a critical parameter to optimize. The V_{GS}=1.0 V is chosen in a way that the channel resistance (3.3 kΩ) in the linear region is close to the resistance of the relevant LRS (3-5 kΩ).

Fig. 6 shows a demonstration of stateful IMPLY using pulses of 100 µs length. V_{COND} and V_{SET} are 0.86 V and 1.1 V respectively. The HRS for logic 0 is programmed in the range of 90-140 kΩ. In input case 4, the current change within the logic pulse period can be clearly observed for both bits *p* and *q*. The *q* bit is set to the LRS within the first 40 µs causing a sudden current increase to another stable state. Concurrently, the current over *p* decreases owing to reduced voltage that results from the fact that the transistor takes over a much larger portion of the voltage drop in the system. Hence, *p* remains in the HRS while *q* is set to the LRS, leading to the logic output of (*p'*/*q'*=0/ 1). For the three other input cases, the stable transient currents observed for the *p* and *q* bits indicate no switching in resistive states. In-line with the truth table of IMPLY, the outputs remain equal to the inputs.

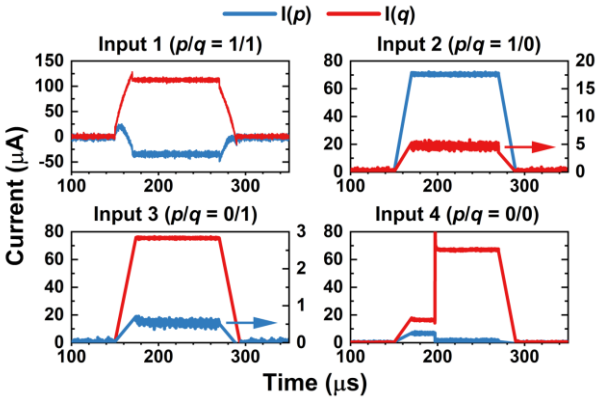


Fig. 6: Transient pulse measurement in active configuration (1T-2R) under different inputs for the stateful IMPLY logic. For input, HRS and LRS of the TaO_x VCM cell are 90-140 kΩ and 3-5 kΩ, respectively. The voltage pulse has a length of 100 µs, where V_{GS} = 1 V, V_{SET} = 1.1 V, and V_{COND} = 0.86 V.

When D2D variability of the VCM cell comes into play, the SET voltage difference is experimentally observed from the two cells used in this IMPLY logic study. According to the distribution function of the SET voltage shown in Fig. 7, the two cells have a 0.186 V difference in the mean SET voltage. This variability can be further experimentally exploited to ease the constraints of the operating voltages. For the IMPLY

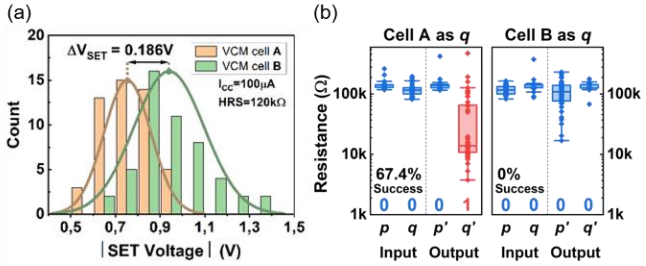


Fig. 7: Effect of D2D SET voltage variability on the success rate of the IMPLY logic. Distribution functions of SET voltage for two TaO_x VCM cells show a 0.186 V difference of their mean values (a). The SET voltages are extracted from 50 bipolar sweep measurements for each cell where the compliance current (I_{CC}) and the HRS were set to 100 µA and 120 kΩ, respectively. The resistance box plot of *p* and *q* presents the comparison of the success rates (b). The most critical input case, (*p*/*q*=0/0), appears when different cells are used as the Q bit. Input of logic 0 (HRS) is 90 - 140 kΩ and the voltage pulse has a length of 100 µs, where V_{GS} = 1 V, V_{SET} = 1.1 V, and V_{COND} = 0.86 V.

stateful logic, only *q* involves resistive switching. It solely occurs under input case four and in the form of a SET operation. In order to enable setting *q*, V_{SET} applied on *q* must be higher than a certain level. On the other hand, *p* has to retain its resistive state. The V_{COND} applied on *p*, therefore, needs to be low enough to avoid a SET in the *p* bit. This can be exploited in a strategic way. When the cell with lower SET voltage is assigned as *q* bit, on which V_{SET} is applied during logic operation, there is an absolute advantage in comparison with the opposite case. Taking the most critical case four, as a decisive example, a comparison of success rates is shown in Fig. 7. When the cell with lower SET voltage is employed as the *q* bit, the success rate of 67.4 % is pronouncedly higher than the 0 % of the opposite scenario.

In contrast to the intentional use of the D2D variability for performance boost, there is another reliability perspective that draws attention to the negative impact from the variability. When two random cells in an array are assigned as *p* and *q* bits, the variability of SET voltage leads to an unfavorable variability of success rates. As a result, the overall success rate over the whole array is diminished. Depending on the application scenario, the SET variability can either be utilized or eliminated.

The importance of D2D variability can also be shown through simulation as shown in Fig. 8 which compares the percentages of stable inputs (a) and correct outputs (b) for different amounts of D2D variability for the 4 different input cases. The percentages are used to calculate the minimum and maximum values of the variability parameters in Table I. For these simulations, we randomly initialized 100 combinations of *p* and *q* for every input case. For comparability with the measurements in section IV, we chose the same pulse widths, SET and COND voltages, and LRS and HRS ranges. The transistor was chosen as described in section II *B*. As expected for input case four (*p*/*q*=1/1) the success rate decreases with increasing D2D variability.

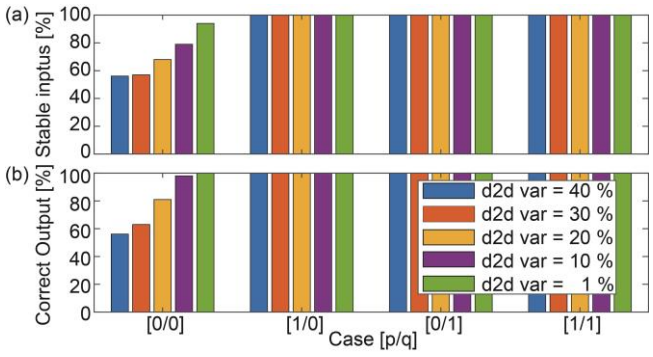


Fig. 8: Impact of the amount of D2D variability on the percentages for stable inputs (a) and correct outputs (b) for the four different input combinations. For Case 4 (*p*/*q*=0/0) the success rates decrease with increasing D2D variability. For the other cases input stability and correct outputs can be achieved independent of the d2d variability.

CONCLUSION

In this work, we have experimentally explored the IMPLY logic operation in passive line arrays and in 1T-nR configurations. The importance of the D2D variability is highlighted and systematically explained by the experiment and simulation. Our results show that exploiting the D2D variability greatly increases the success rate of IMPLY logic, while using a random assignment of *p* and q devices leads to a reduced success rate due to the D2D variability.

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