

Qubit bias using a CMOS DAC at mK temperatures

Rene Otten, Lea Schreckenberg, Patrick Vliex, Julian Ritzmann, Arne Ludwig, Andreas D. Wieck & Hendrik Bluhm

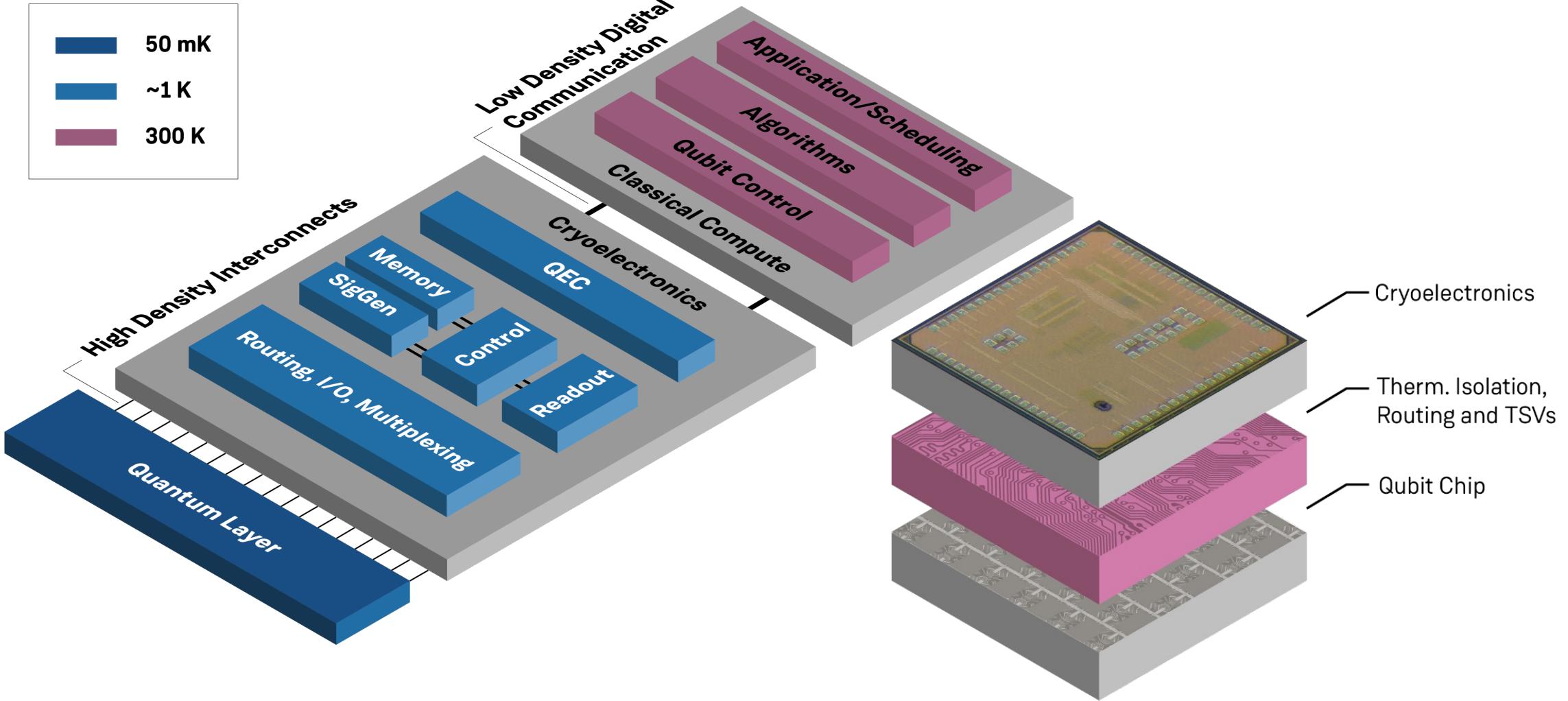
C5L-C



RWTH AACHEN
UNIVERSITY

JÜLICH
Forschungszentrum

Introduction



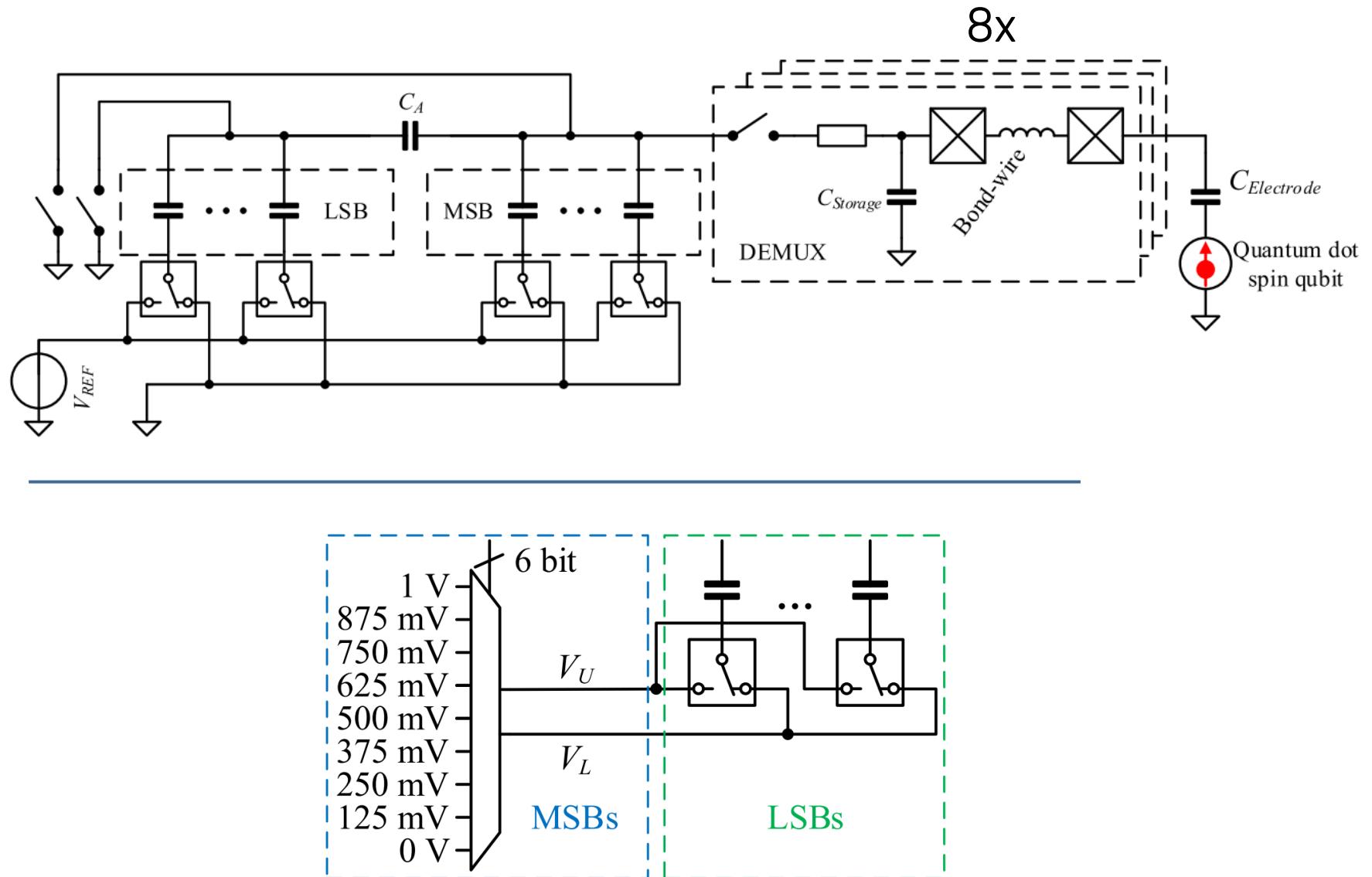
Fully Autonomous DC Bias-DAC Operating at <50mK

See also

- Pauka, S.J., Das, K., Kalra, R. et al. Nat Electron (2021)
Xue, X., Patra, B., van Dijk, J.P.G. et al. Nature (2021)

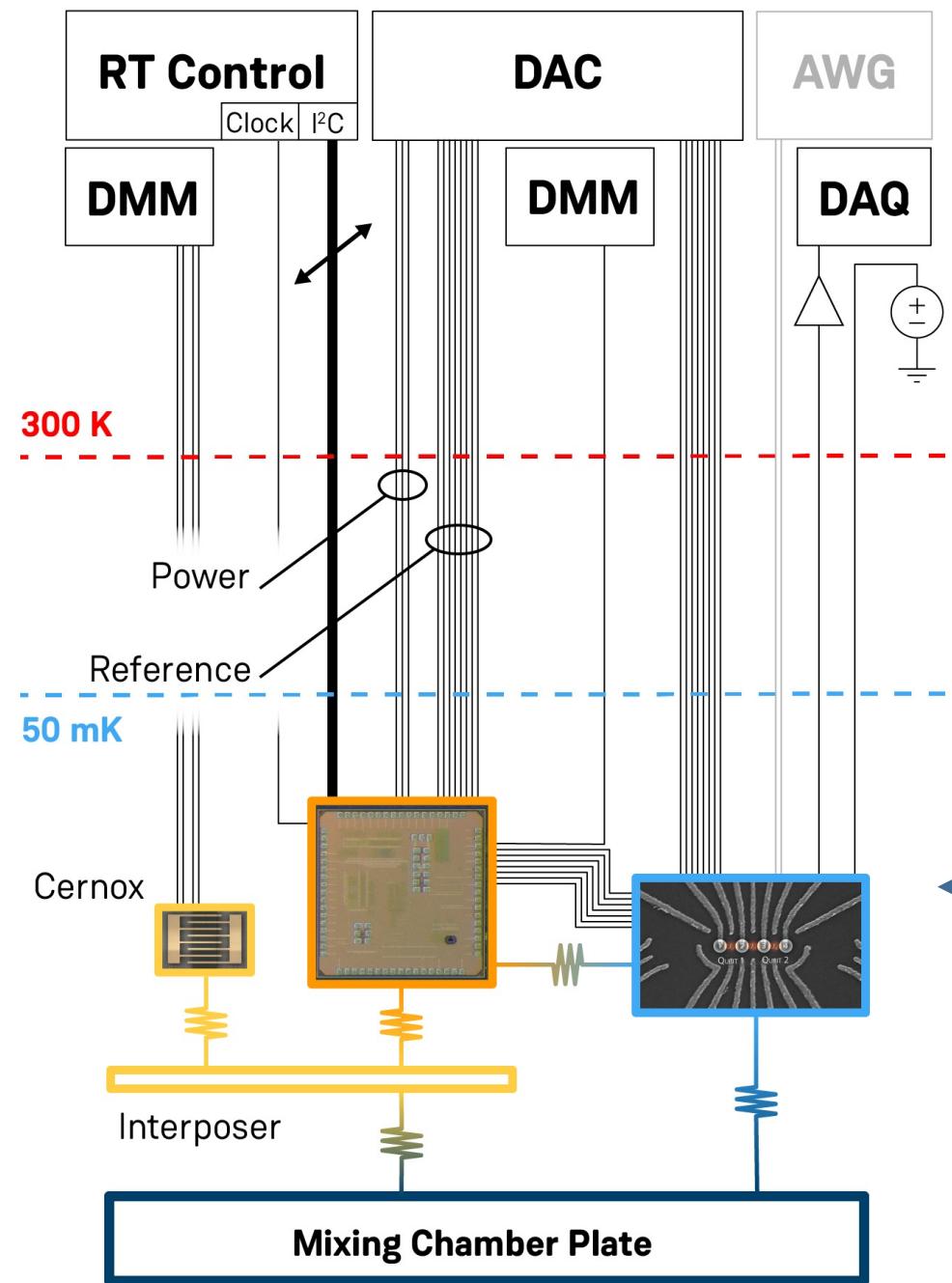
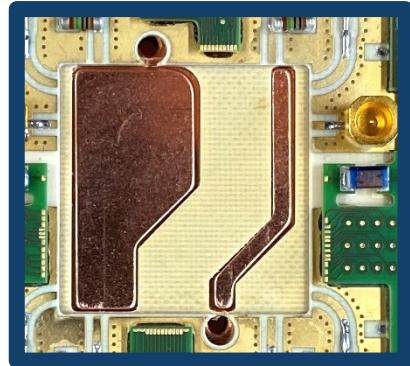
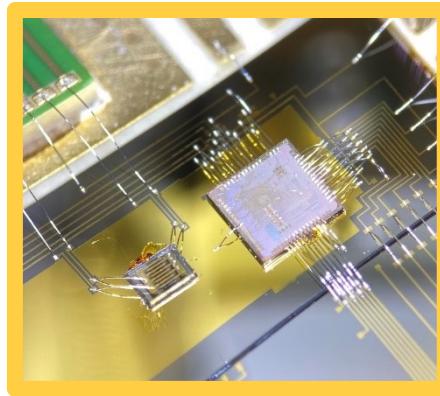
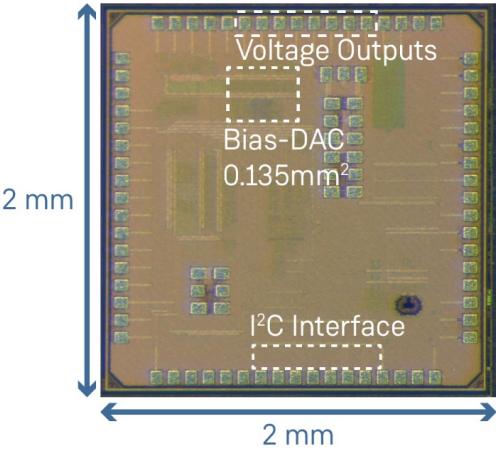
DAC Architecture & Design Considerations

Process	65 nm CMOS
Resolution	13 bit
Range	0 - 1 V
Power Consumption	< 400 μ W

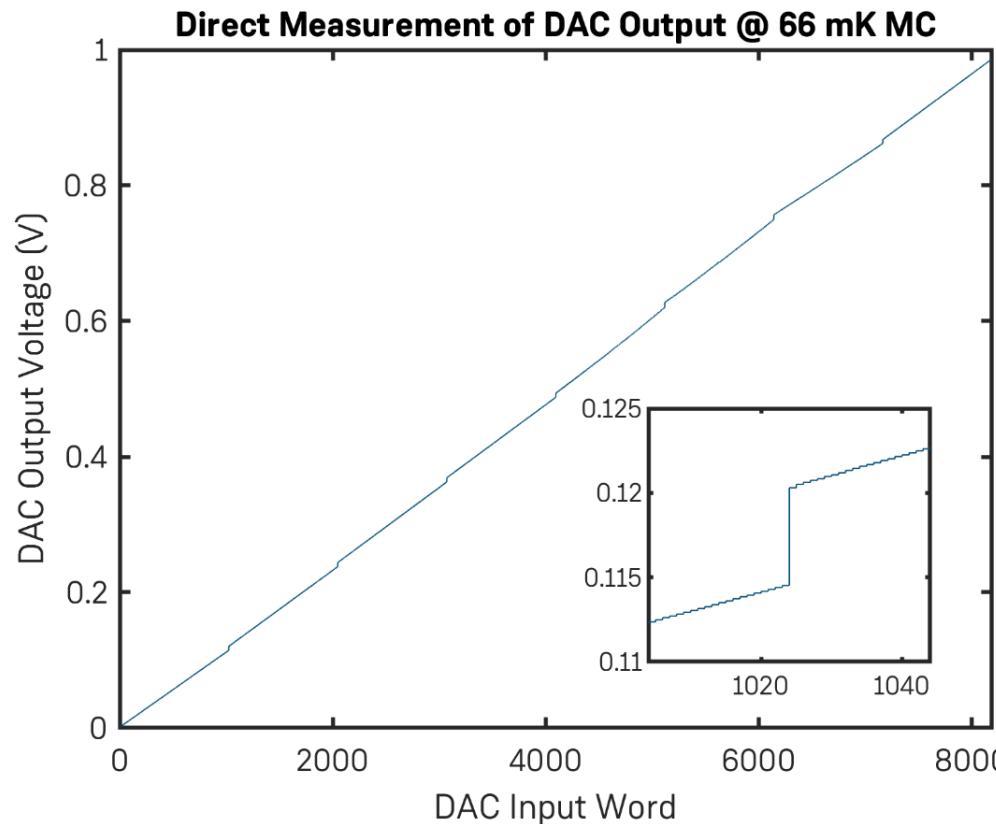


P. Vliex et al., IEEE SSC Letters, vol. 3, 2020, pp. 218–221.

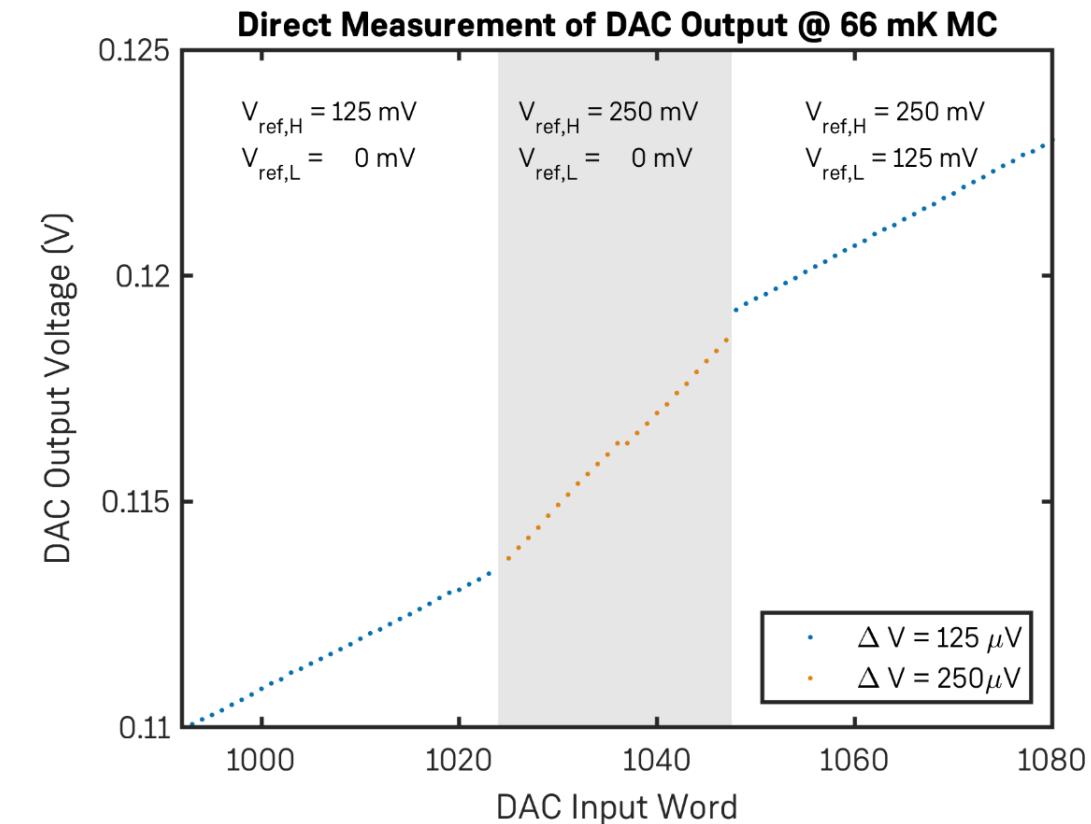
Cryostat Wiring



Direct DAC Output Voltage Characterization

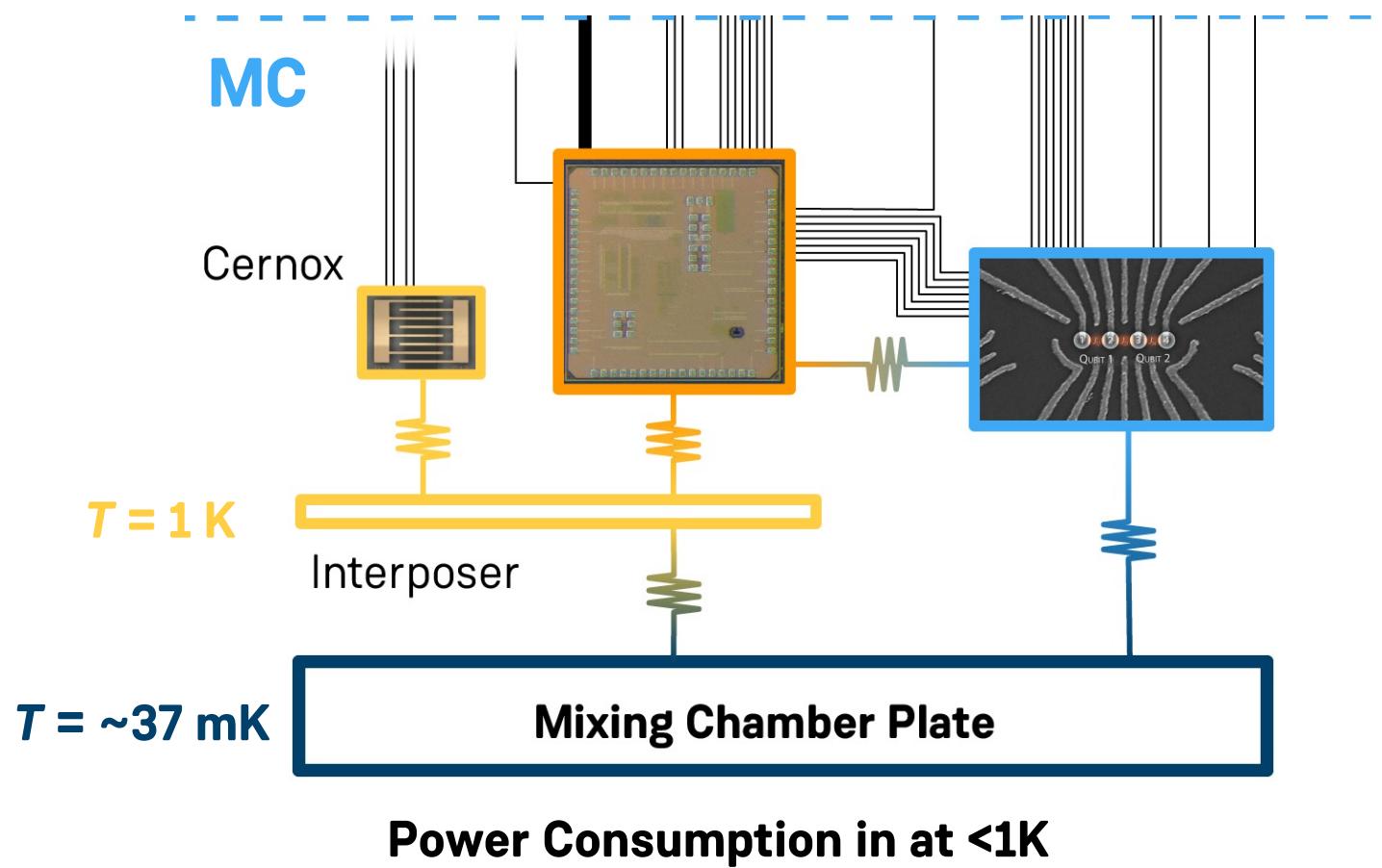


*Stray capacitances lead to
gain error*



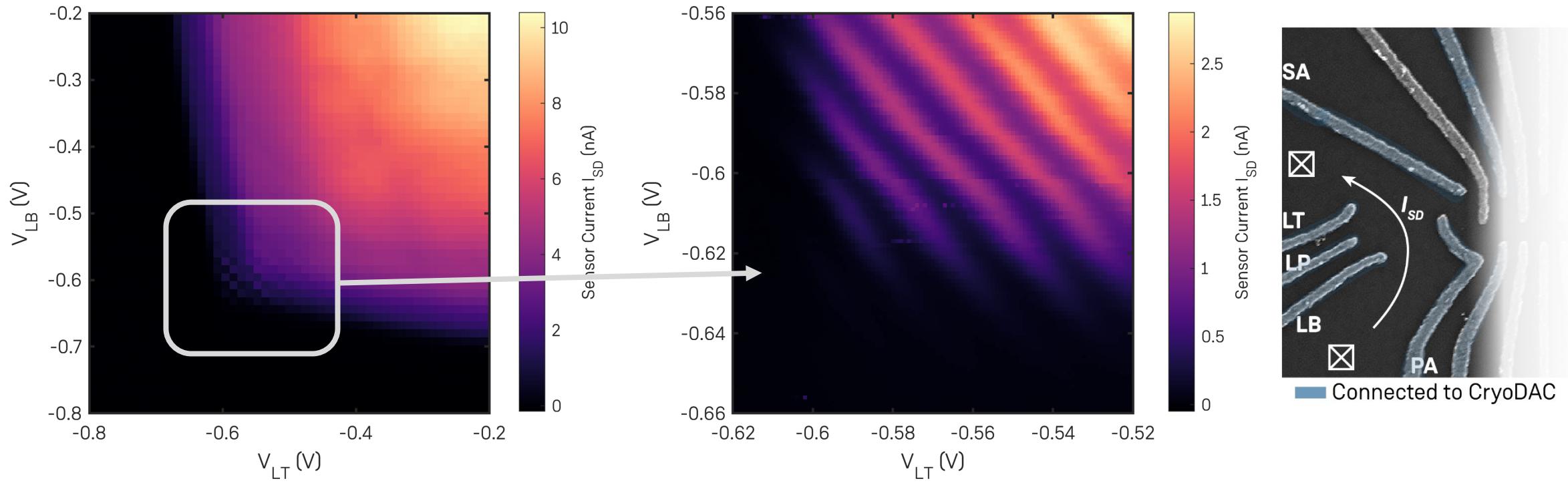
*We can bridge these gaps by
overlapping reference
voltages*

DAC Temperature & Power Consumption

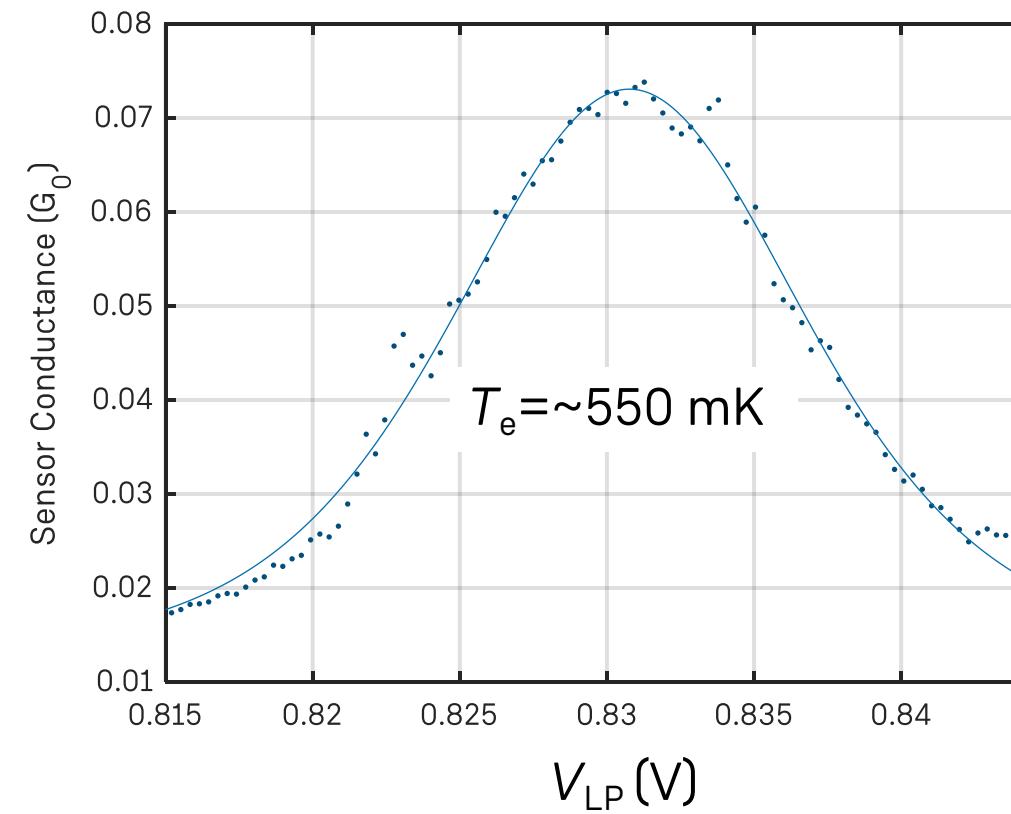
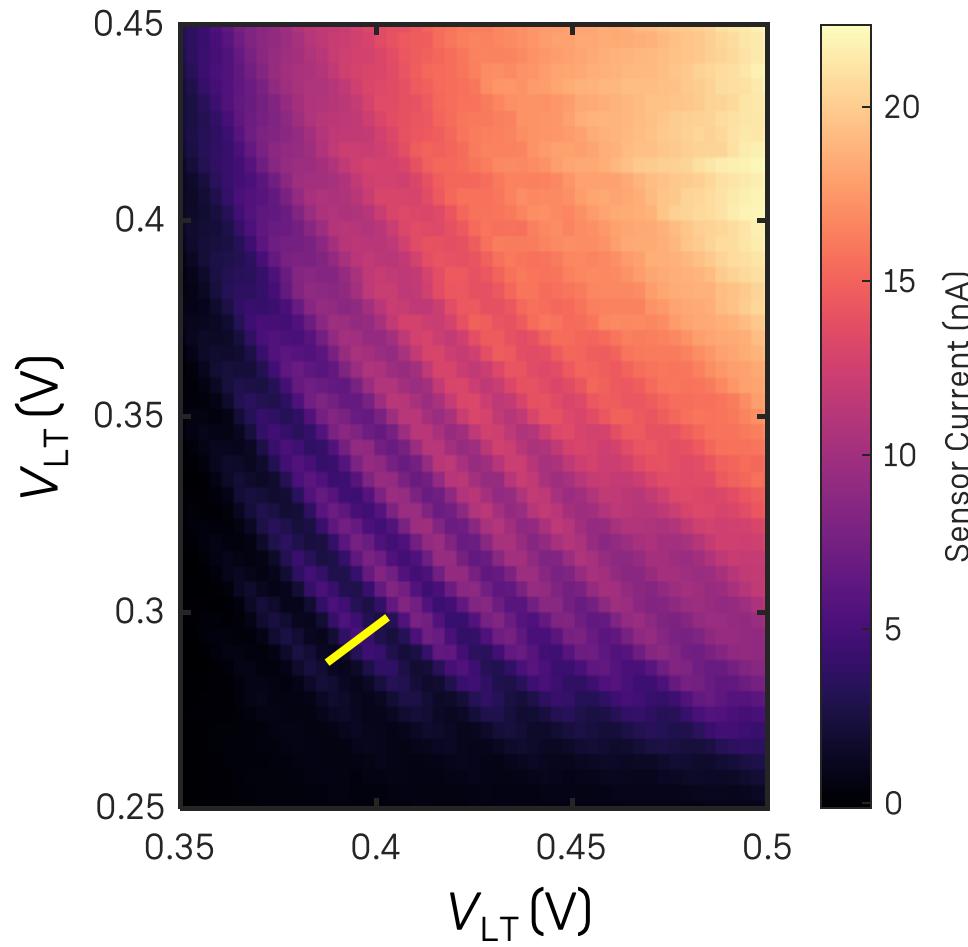


$$\begin{aligned} P_{\text{all}} &\sim 30 \mu\text{W} (\text{I}^2\text{C}, 10 \text{ MHz Clock, DAC}) \\ P_{\text{DAC}} &\sim 13 \mu\text{W} \end{aligned}$$

Sensor Dot Measurement using Cryo-DAC

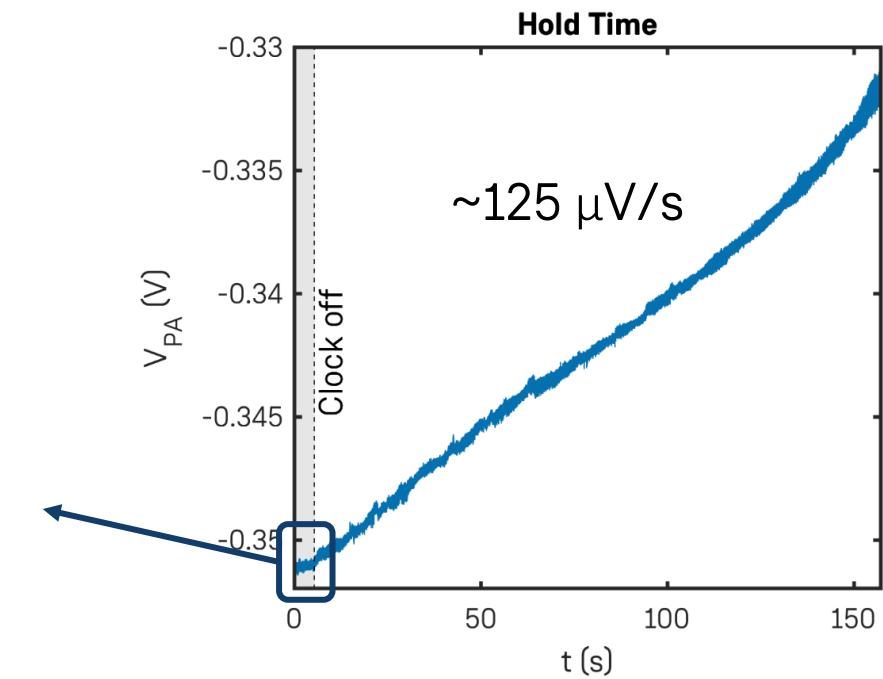
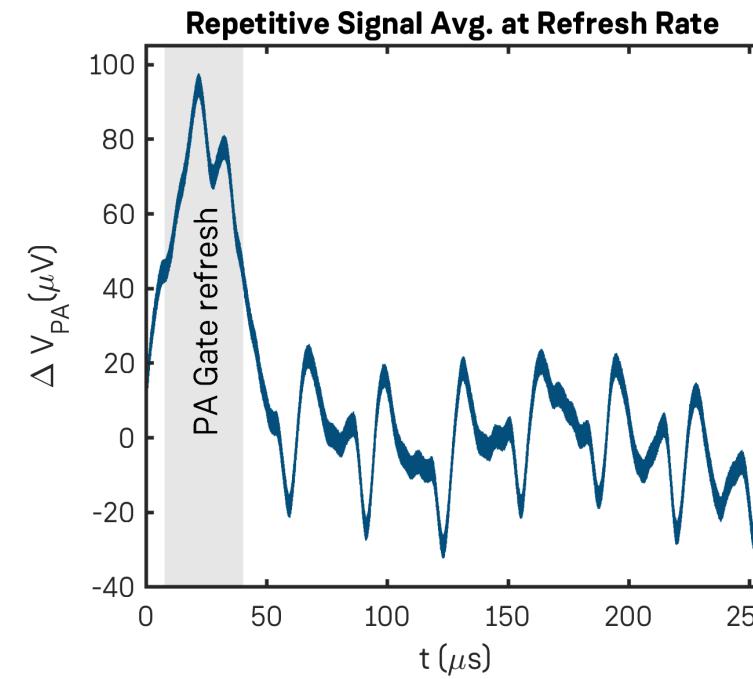
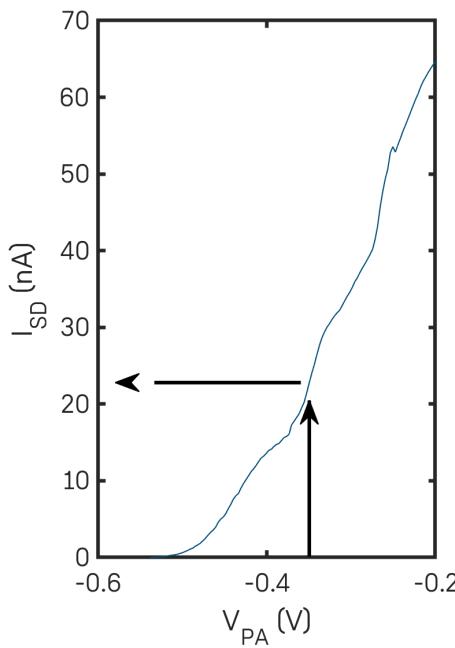
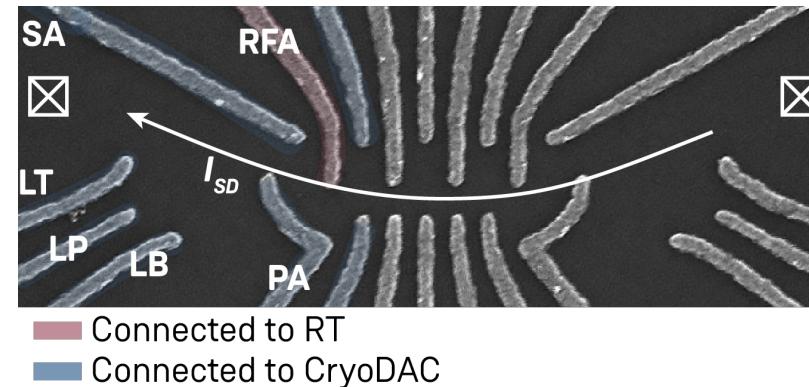


Coulomb Diamonds und Electron Temperature



$$G = \frac{G_0}{\cosh^2 \left(\frac{\alpha_{LP}(V_{LP} - V_0)}{2k_B T_e} \right)}.$$

DAC Voltage Stability



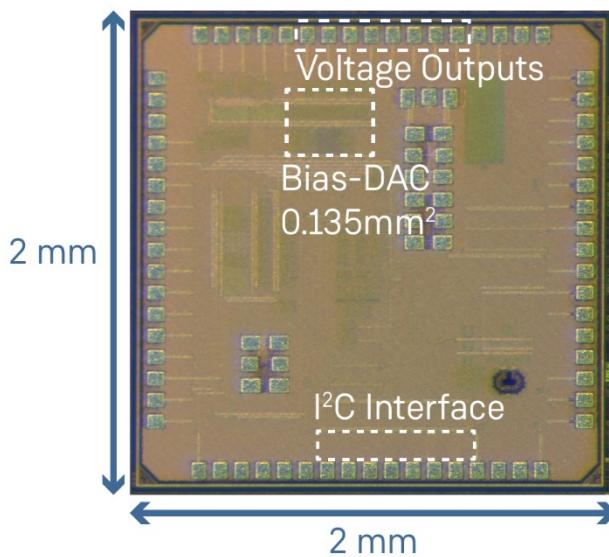
10 Hz Gate Refresh
~3000 gates per cycle



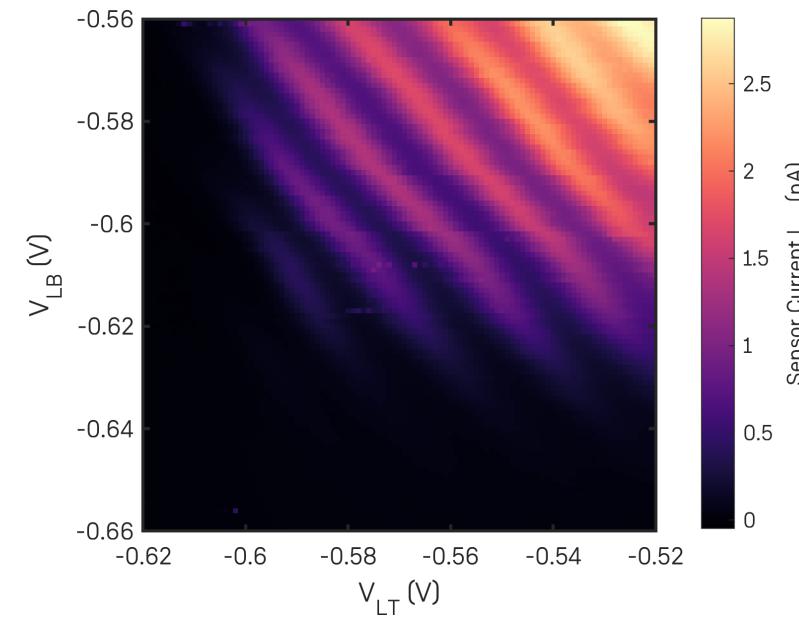
13 μ W DAC Power
4 nW per channel

Conclusion

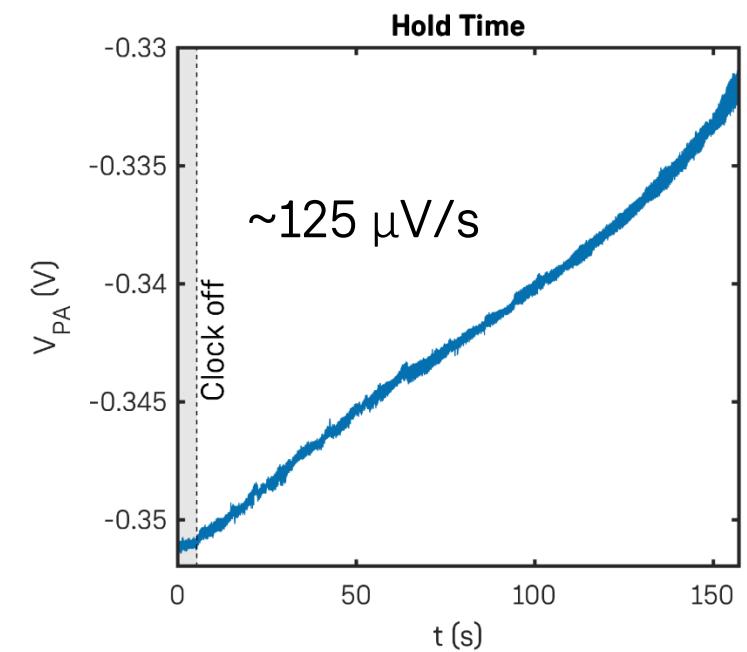
CryoDAC
Operating at <50 mK



First Measurements on
Qubit Device



Low Operating
Frequencies Possible



Fully Autonomous DC Bias-DAC Operating $T_{MC} = 37\text{mK}$

Thank you!

ZEA-2/FZJ

Lea Schreckenberg

Patrick Vliex

Ruhr Universität Bochum

Julian Ritzmann

Arne Ludwig

Andreas D. Wieck

RWTH Aachen University

Matthias Künne

Simon Humpohl

Hendrik Bluhm

We are looking for Postdocs!

