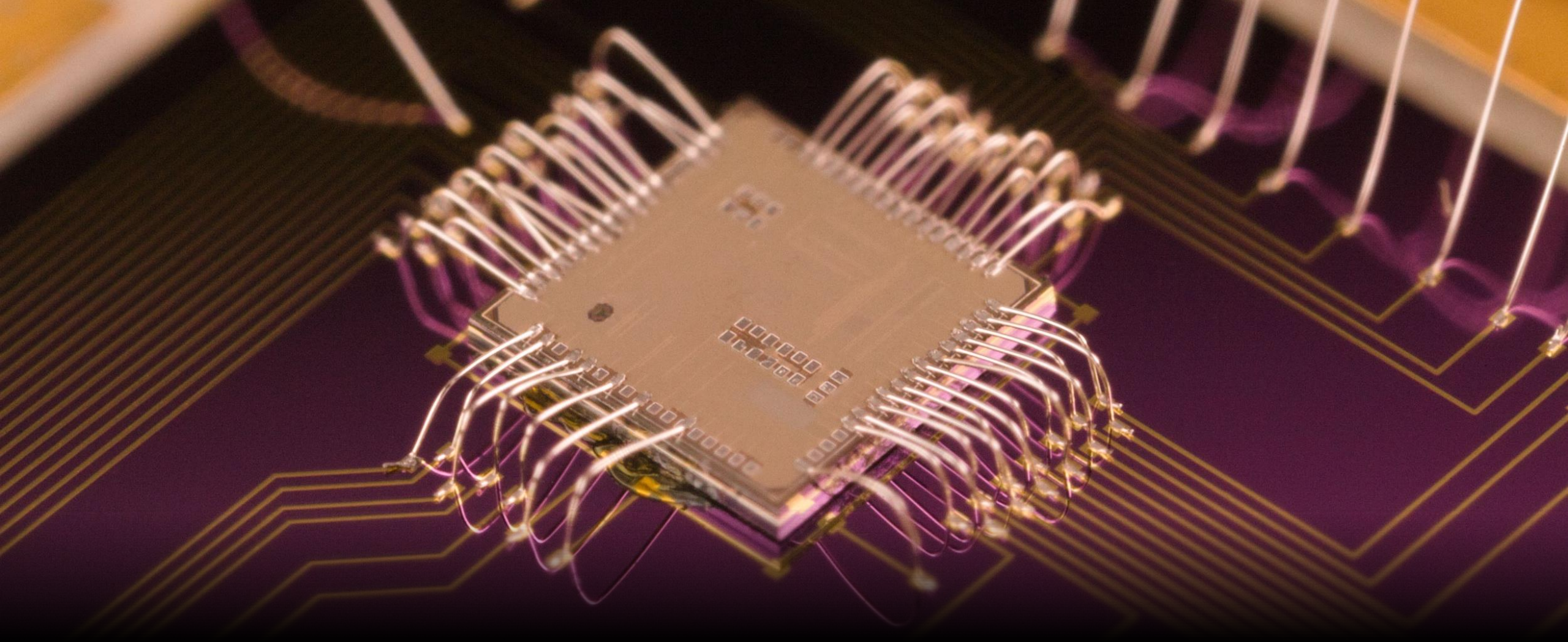


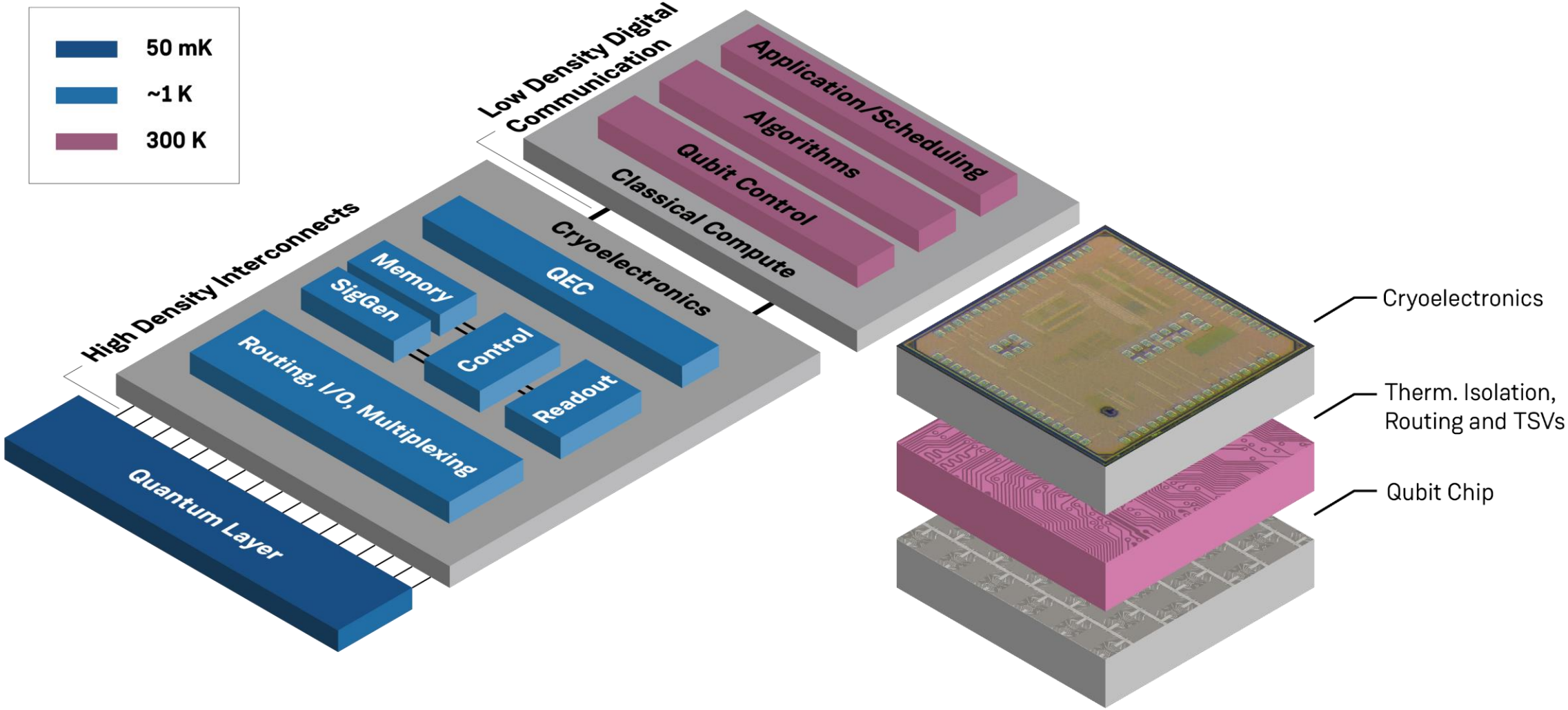
Qubit bias using a CMOS DAC at mK temperatures

Rene Otten, Lea Schreckenberg, Patrick Vliex, Julian Ritzmann, Arne Ludwig, Andreas D. Wieck & Hendrik Bluhm

A39.00009

Quantum Technology Group | RWTH AACHEN UNIVERSITY | JÜLICH Forschungszentrum

Introduction



Fully Autonomous DC Bias-DAC Operating at 45mK

Abstract: A39.00009 : Qubit bias using a CMOS DAC at mK temperatures

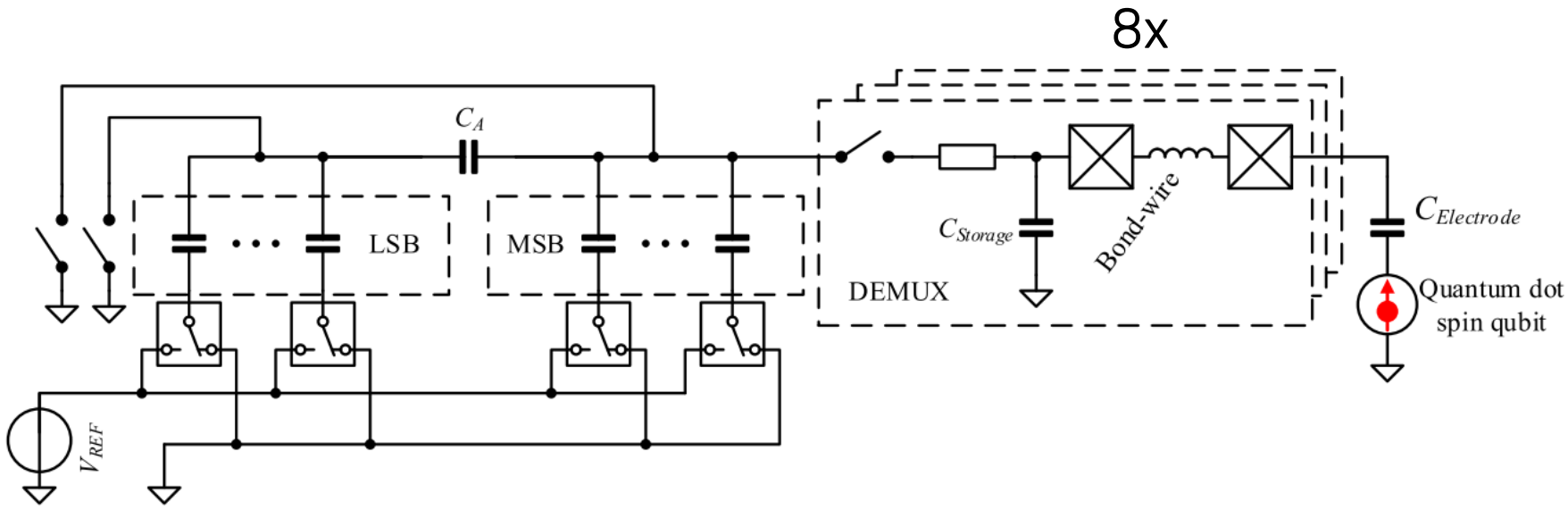
See also

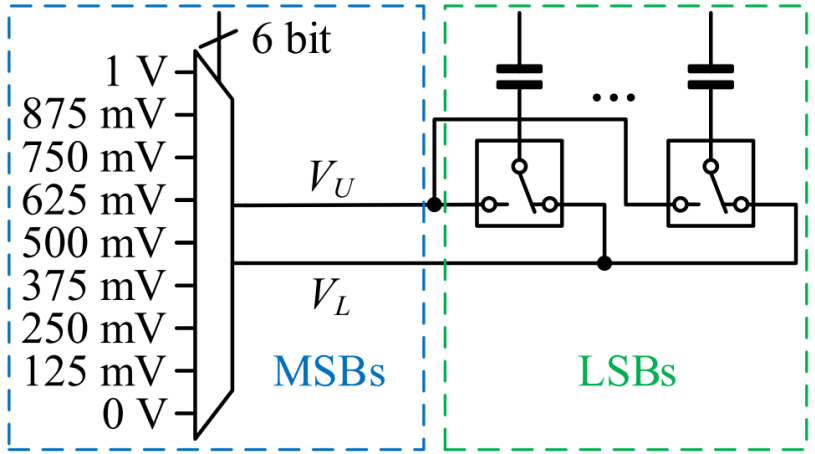
Pauka, S.J., Das, K., Kalra, R. et al. Nat Electron (2021)

Xue, X., Patra, B., van Dijk, J.P.G. et al. Nature (2021)

DAC Architecture & Design Considerations

Process	65 nm CMOS
Resolution	13 bit
Range	0 – 1 V
Power Consumption	< 400 µW

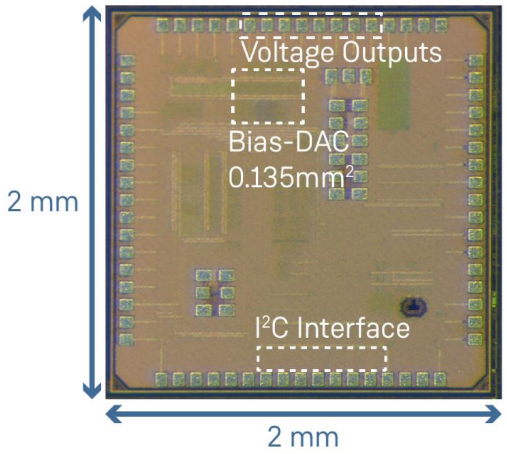


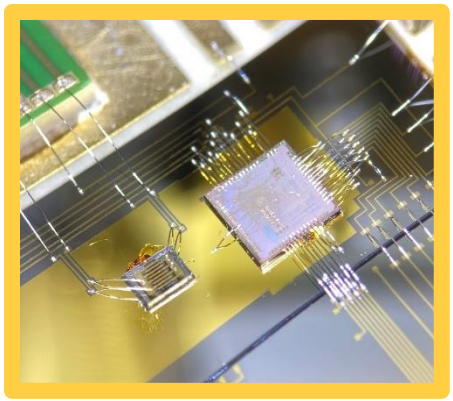


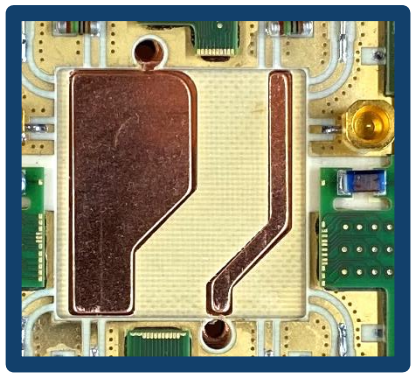
Abstract: A39.00009 : Qubit bias using a CMOS DAC at mK temperatures

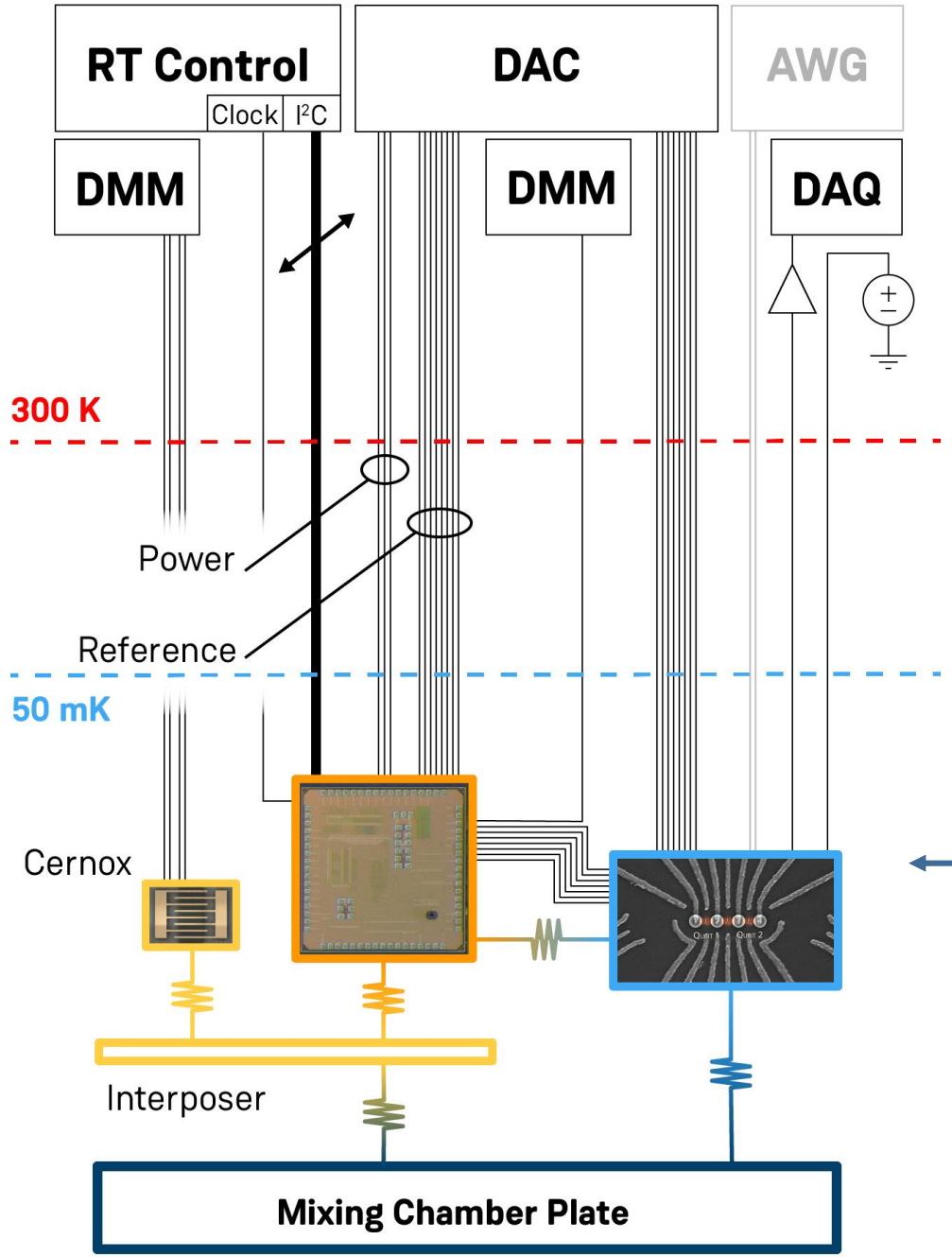
P. Vliex et al., IEEE SSC Letters, vol. 3, 2020, pp. 218–221.
Lotte Geck et al. 2020 Quantum Sci. Technol. 5 015004

Cryostat Wiring





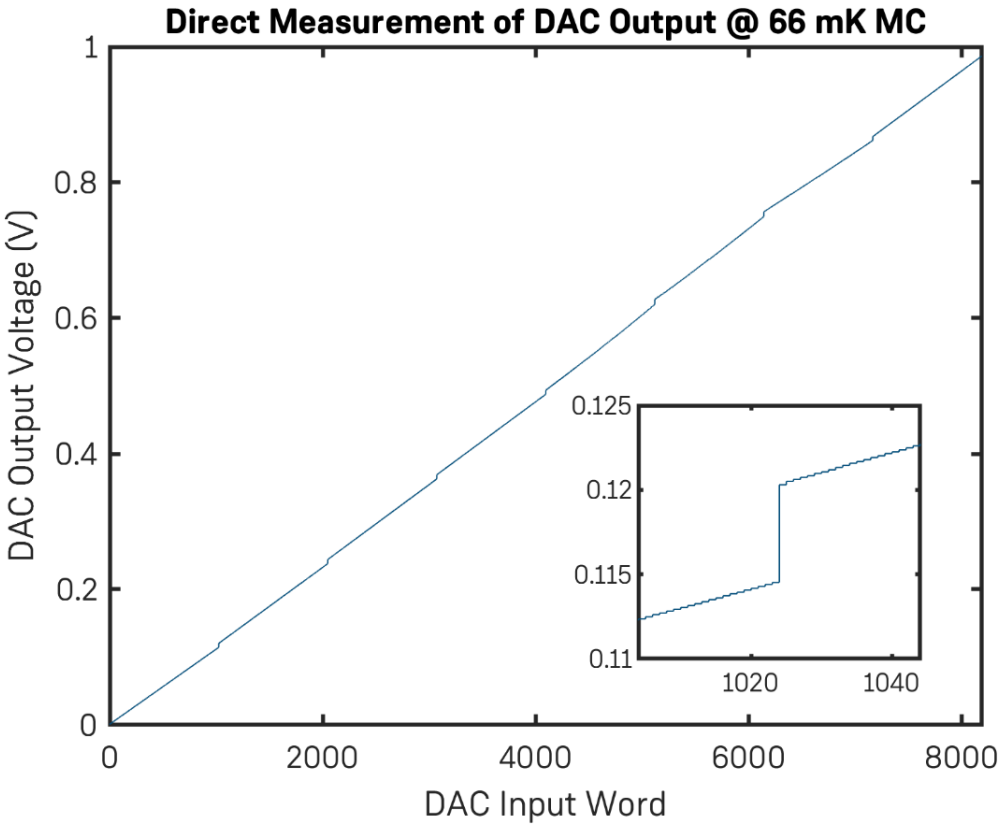




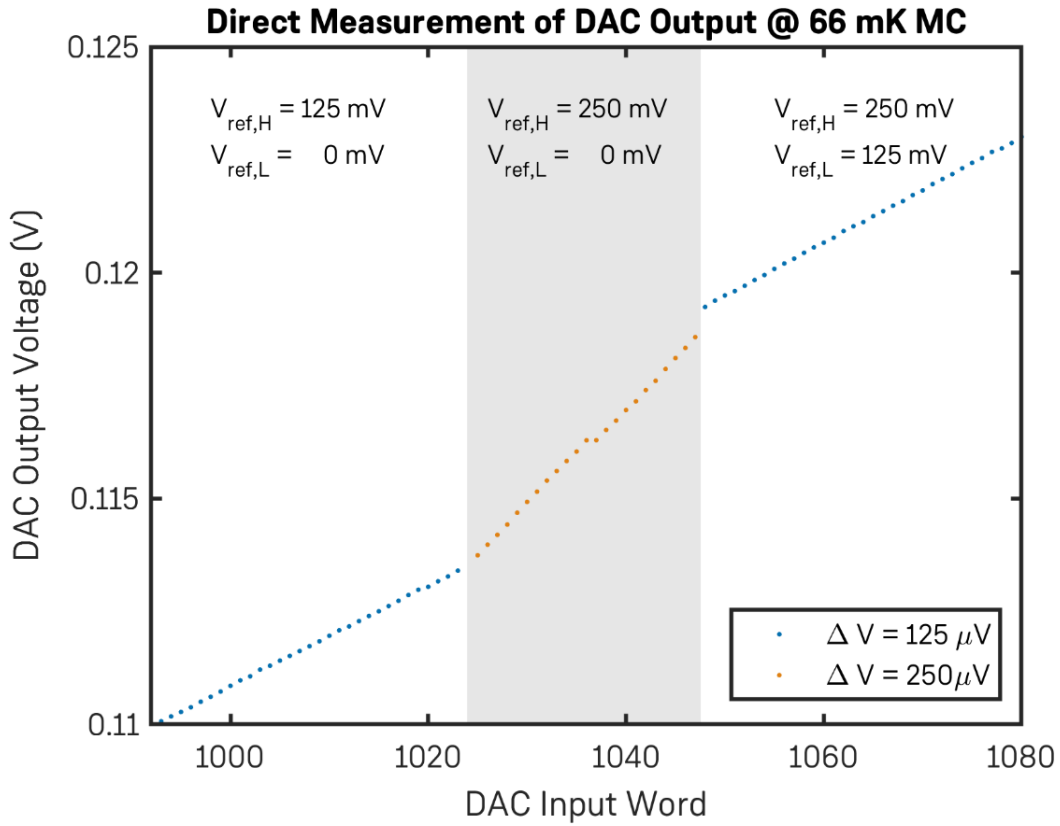
Abstract: A39.00009 : Qubit bias using a CMOS DAC at mK temperatures

JÜLICH Forschungszentrum

Direct DAC Output Voltage Characterization



Stray capacitances lead to gain error

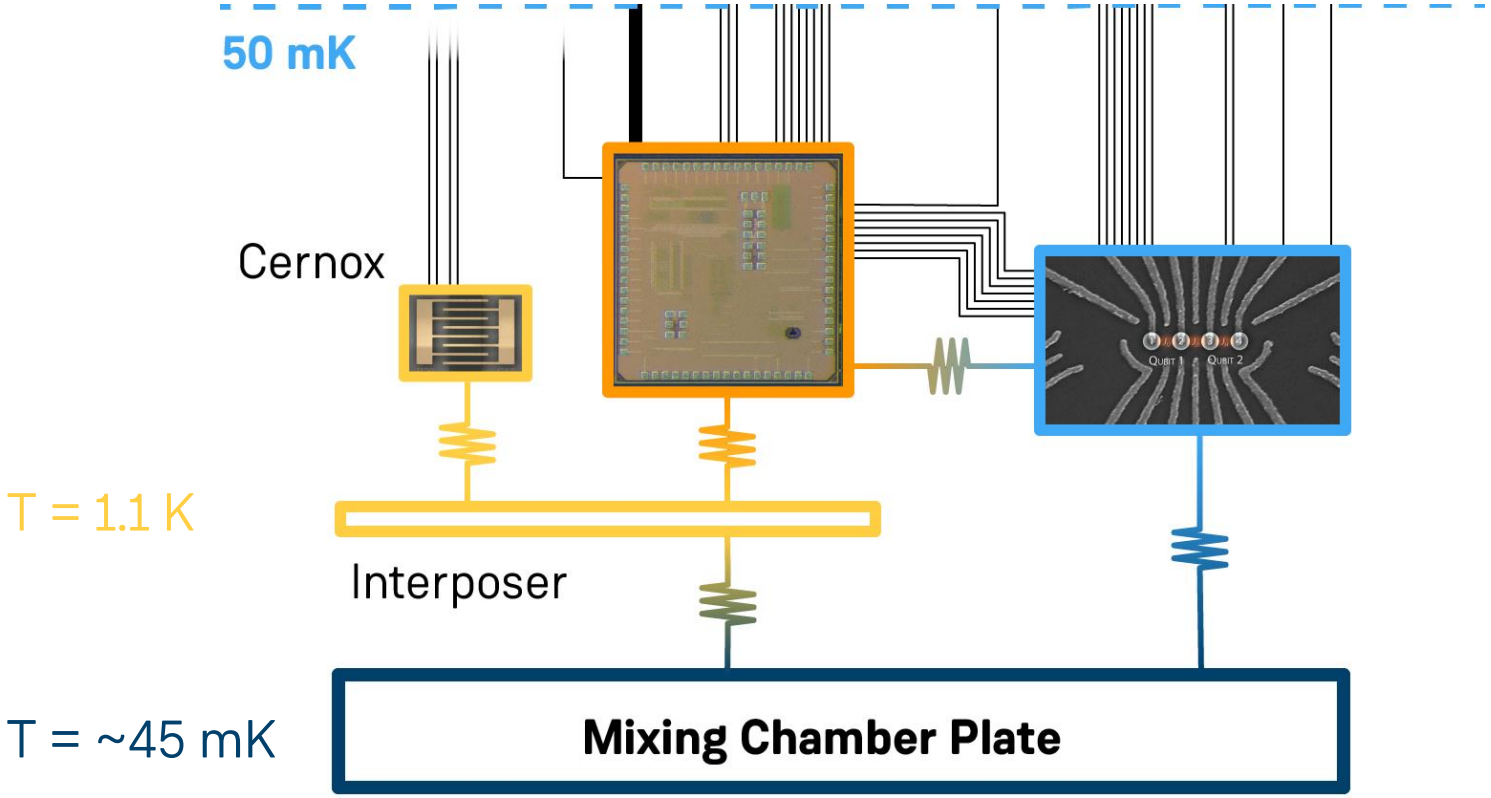


We can bridge these gaps by overlapping reference voltages

Abstract: A39.00009 : Qubit bias using a CMOS DAC at mK temperatures

JÜLICH Forschungszentrum

DAC Temperature & Power Consumption



Power Consumption

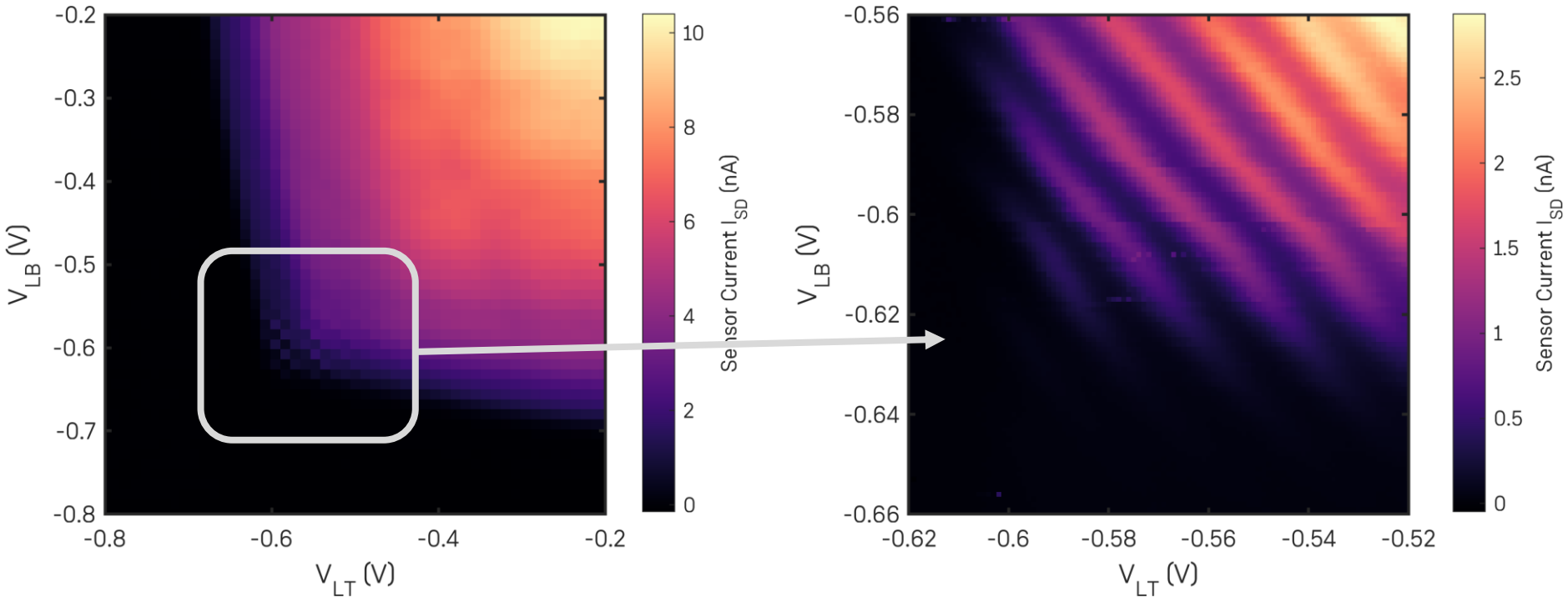
P_{all} ~47 µW (I^2C, 10 MHz Clock, DAC)

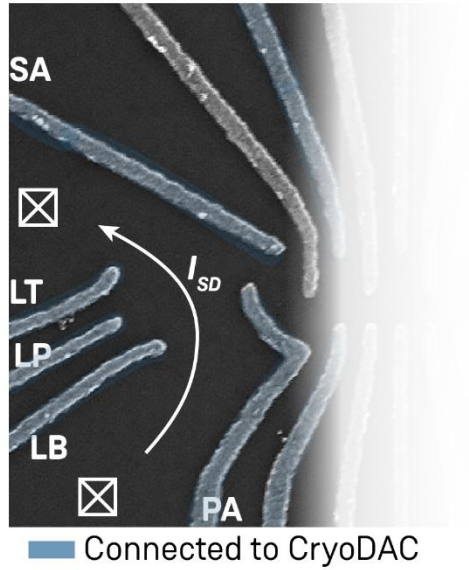
From Previous Measurements

P_{DAC} ~20 µW

Abstract: A39.00009 : Qubit bias using a CMOS DAC at mK temperatures

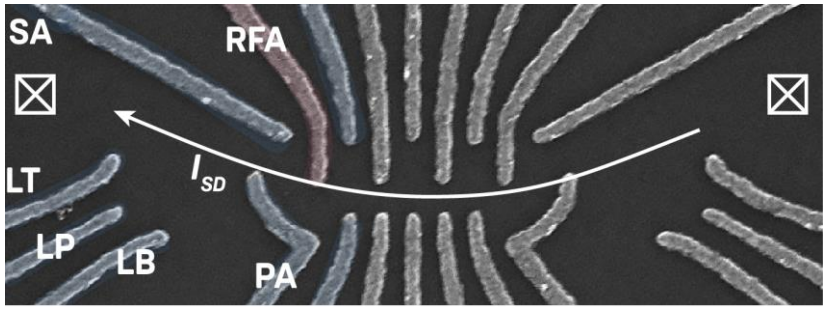
Sensor Dot Measurement using Cryo-DAC

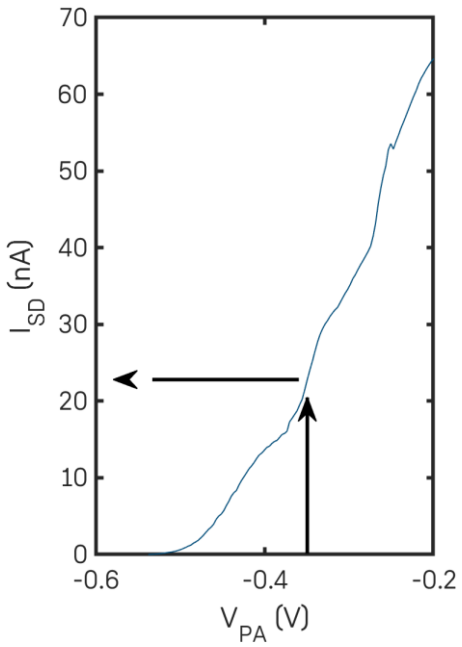


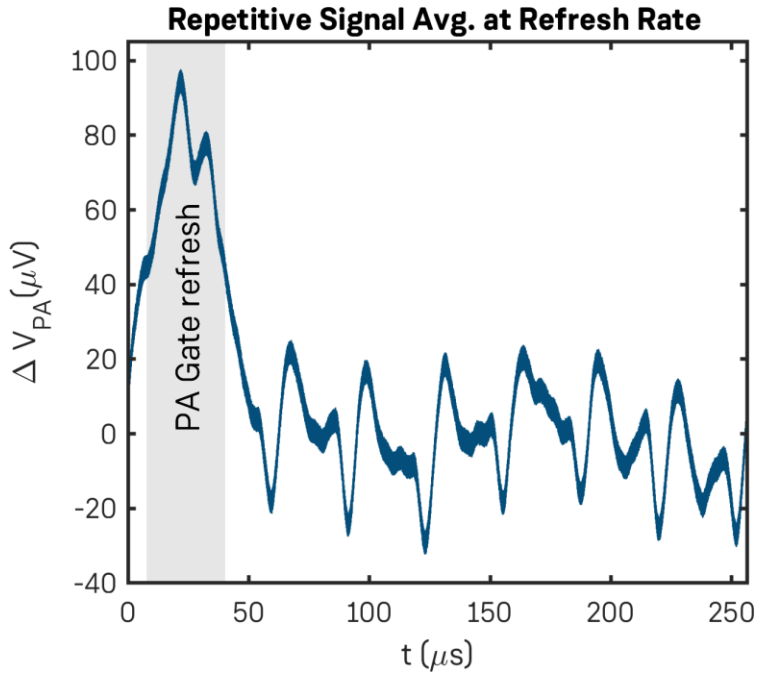


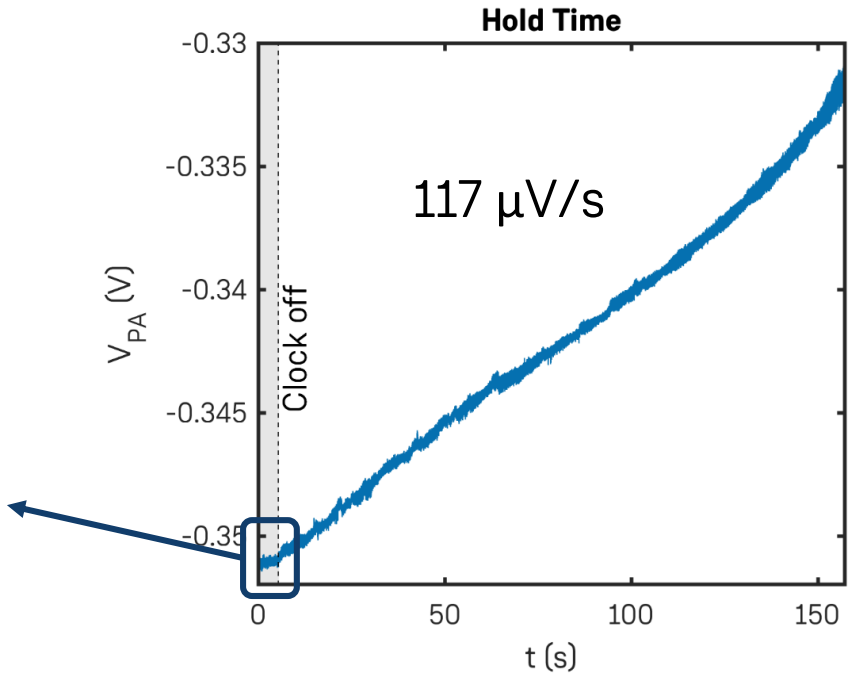
Abstract: A39.00009 : Qubit bias using a CMOS DAC at mK temperatures

DAC Voltage Stability









10 Hz Gate Refresh
3125 gates per cycle

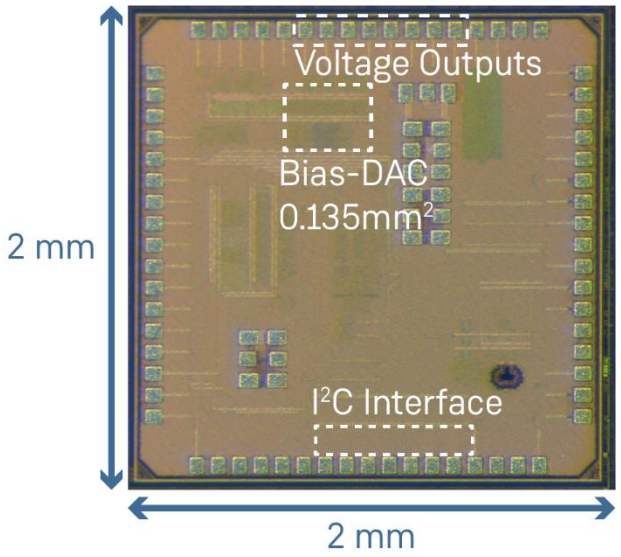
20 µW DAC Power
6 nW per channel

Abstract: A39.00009 : Qubit bias using a CMOS DAC at mK temperatures

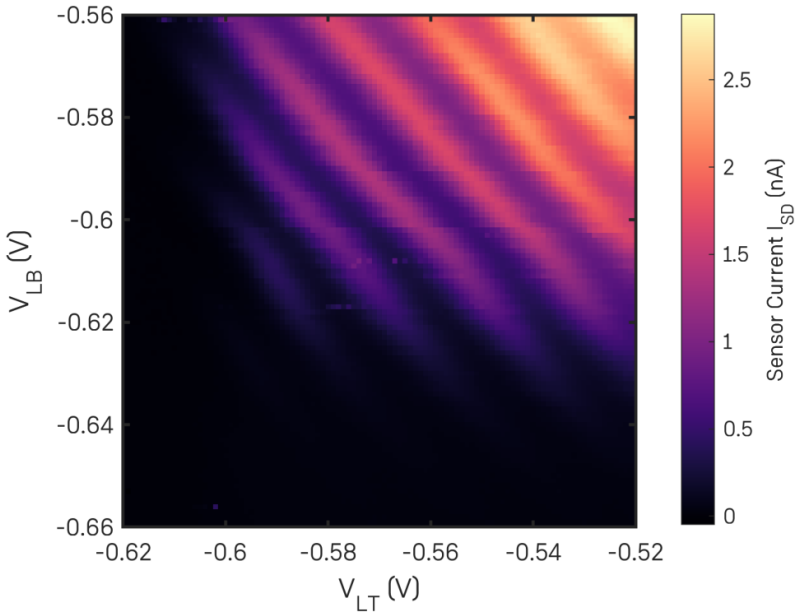
JÜLICH Forschungszentrum

Conclusion

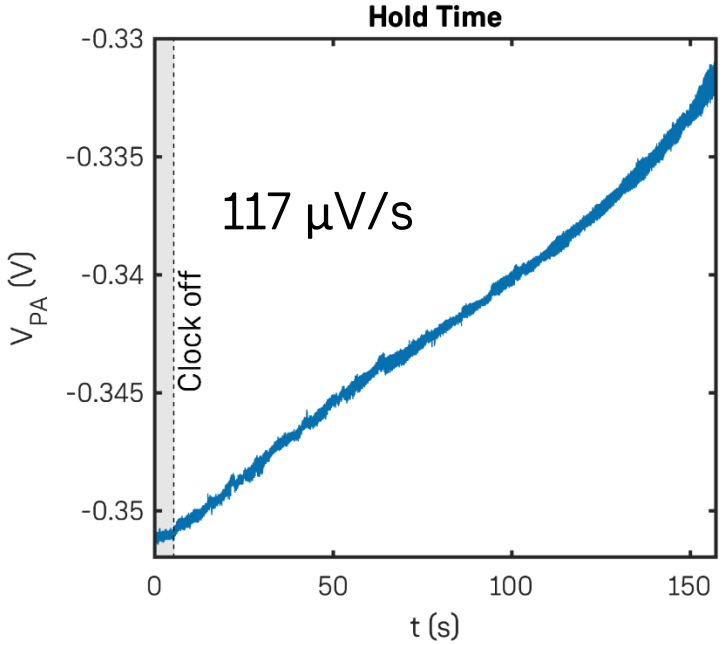
CryoDAC
Operating at 45 mK



First Measurements on
Qubit Device



Low Operating
Frequencies Possible



Fully Autonomous DC Bias-DAC Operating at 45mK

Abstract: A39.00009 : Qubit bias using a CMOS DAC at mK temperatures

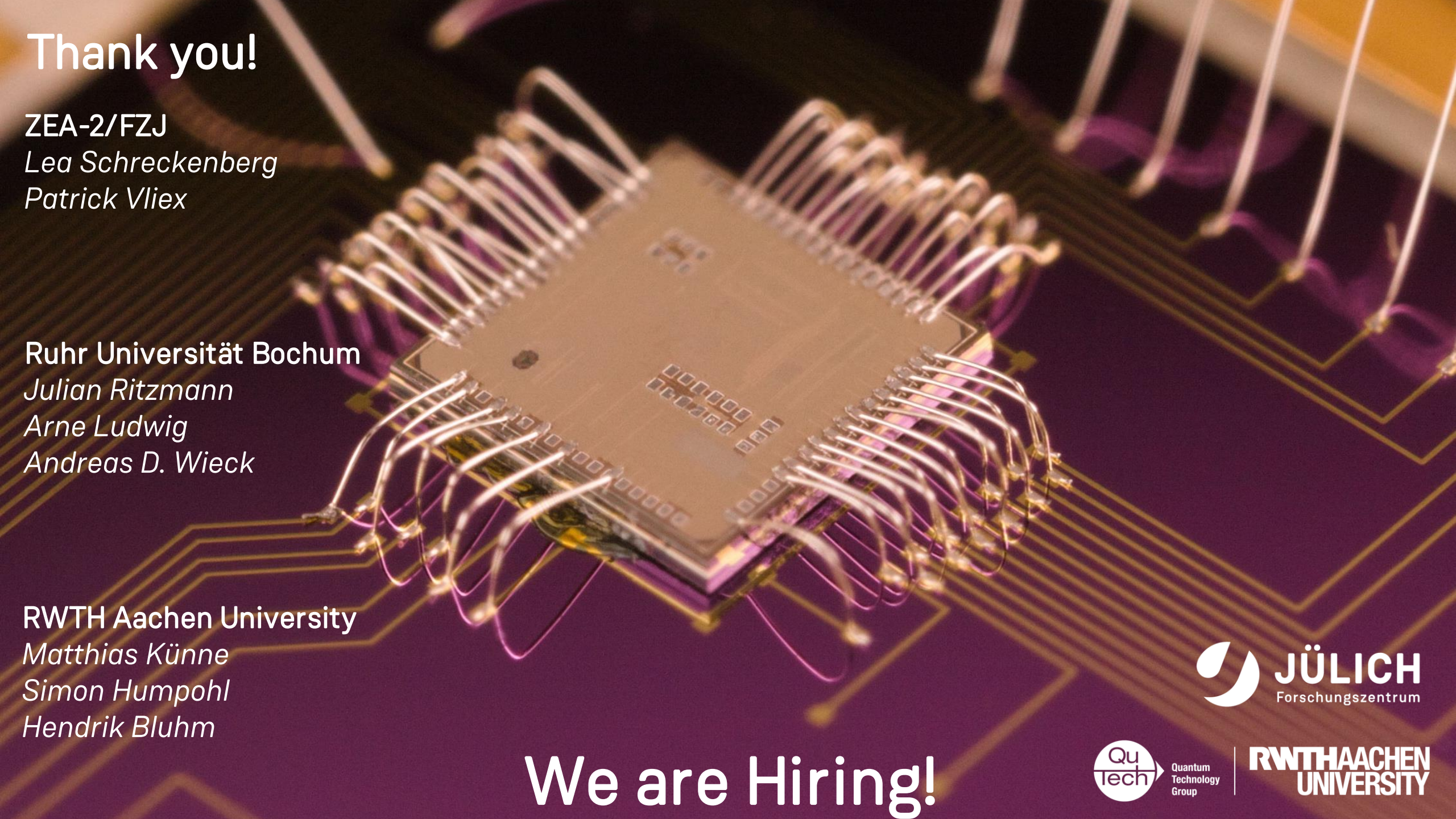
JÜLICH Forschungszentrum

Thank you!

ZEA-2/FZJ
Lea Schreckenberg
Patrick Vliex

Ruhr Universität Bochum
Julian Ritzmann
Arne Ludwig
Andreas D. Wieck

RWTH Aachen University
Matthias Künne
Simon Humpohl
Hendrik Bluhm



JÜLICH Forschungszentrum

Qu Tech Quantum Technology Group | RWTH AACHEN UNIVERSITY

We are Hiring!

Block	Power consumption
Charge-redistribution DAC & multiplexed output channel (ref. to Fig. 5.14)	77 nW
DAC reference voltages, all 8 summed (ref. to Fig. 5.14)	3 nW
DAC digital logic, memory & control (ref. to Fig. 5.14)	21 µW
Bias-DAC total	21.1 µW (2.63 µW per channel)
Clock buffer	4.3 µW
Total	25.4 µW (3.18 µW per channel)