

Qubit Bias using a CMOS DAC at mK Temperatures

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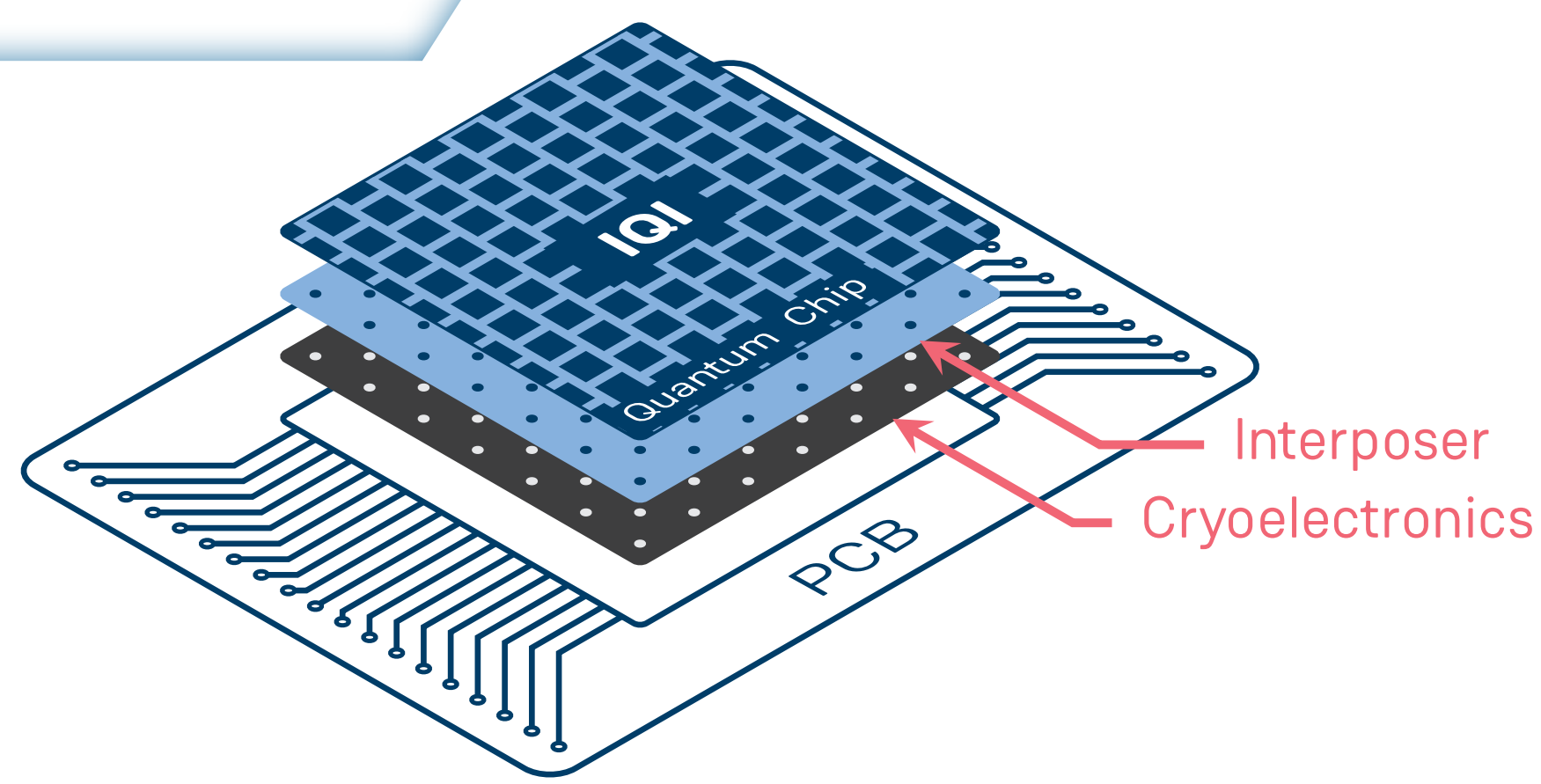
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Abstract

Scaling up a quantum processor to tackle real-world problems requires qubit numbers in the millions. Scalable semiconductor-based architectures have been proposed, many of them relying on integrated control instead of room-temperature electronics. However, it has not yet been shown that this can be achieved. For developing a high-density, low-cost wiring solution, it is highly advantageous for the electronics to be placed at the same temperature as the qubit chip. Therefore, tight integration of the qubit chip with ultra low power complementary metal-oxide-semiconductor (CMOS) electronics presents a promising route. We demonstrate DC biasing qubit electrodes using a custom-designed 65nm CMOS capacitive digital-to-analog converter (DAC) operating on the mixing chamber of a dilution refrigerator below 45 mK. Our chip features a complete proof of principle solution including interface, DAC memory and logic, the capacitive DAC, and sample-and-hold structures to provide voltages for multiple qubit gates. The bias-DAC (CryoDAC) is combined with the qubit using a silicon interposer chip, enabling flexible routing and tight integration. Voltage stability, noise performance, and temperature are benchmarked using the qubit chip. Our results indicate that qubit bias at cryogenic temperatures with a power consumption of 4 nW/ch is feasible with this approach. They validate the potential of very low power qubit biasing using highly integrated circuits whose connectivity requirements do not increase with the number of qubits.

Concept



Scaling to qubit numbers required for quantum error correction requires integration of control electronics and quantum chips [1,8]

- Qubits and electronics are placed in the same package, qubits are operated at the base temperature of a cryostat
- Electronics can be operated at up to 1.8 K where ample cooling power is available (~W)
- Thermal solutions need to be engineered to remove heat and keep qubits at their ideal operating temperature

Novel architectures match the qubits native dimension with the space needed for electronics [2-5]

References

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Qubit Integration

Integrate a CMOS bias-DAC (CryoDAC) with a GaAs qubit chip on the mixing chamber (MC) plate of a dilution refrigerator

- We integrate the two chips on a silicon interposer
- Direct metal contact to MC and a split interposer ensure sufficient thermal anchoring and minimal heatload on the qubit
- IC power of 30 μ W well below fridge cooling power results in 37 mK MC temperature and 0.9K interposer temperature near the IC

Fully autonomous DC biasing DAC operated on the mixing chamber of a dilution refrigerator

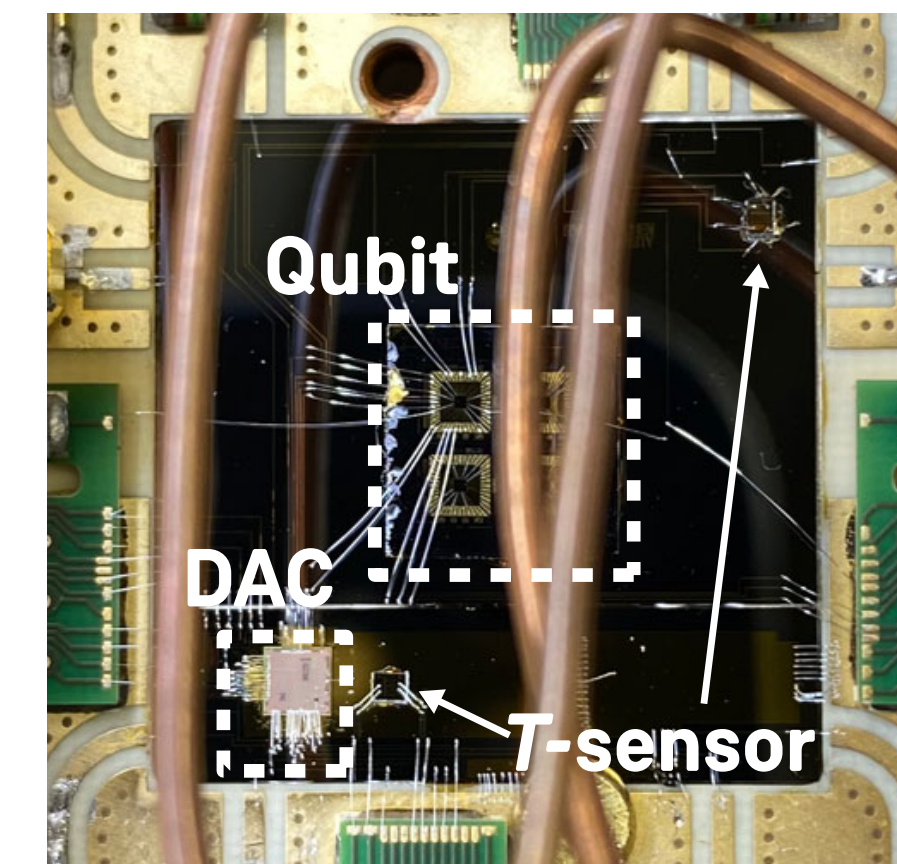


Fig. 1: Picture of the silicon interposer holding both the qubit and IC. The backside is in direct contact with the copper from the mixing chamber to yield sufficient thermal anchoring. The interposer is split to limit direct heating of the qubit from the IC. Wirebonds are used to connect the interposer, qubit and DAC chips. Seven channels from the DAC are connected directly to the qubit gates. One is routed to RT for testing purposes. We place additional temperature sensors on the interposer close to the DAC and qubit.

CryoDAC

TSMC 65 nm CMOS charge-redistribution DAC developed by ZEA-2 [6]

- 13 bit resolution at an output voltage range of 0 - 1 V with 8 channels
- 13 μ W power consumption at 10 MHz clock limited by dynamic dissipation of digital circuitry
- Periodic voltage refresh to counteract (potential) leakage at ~ 3.8 kHz

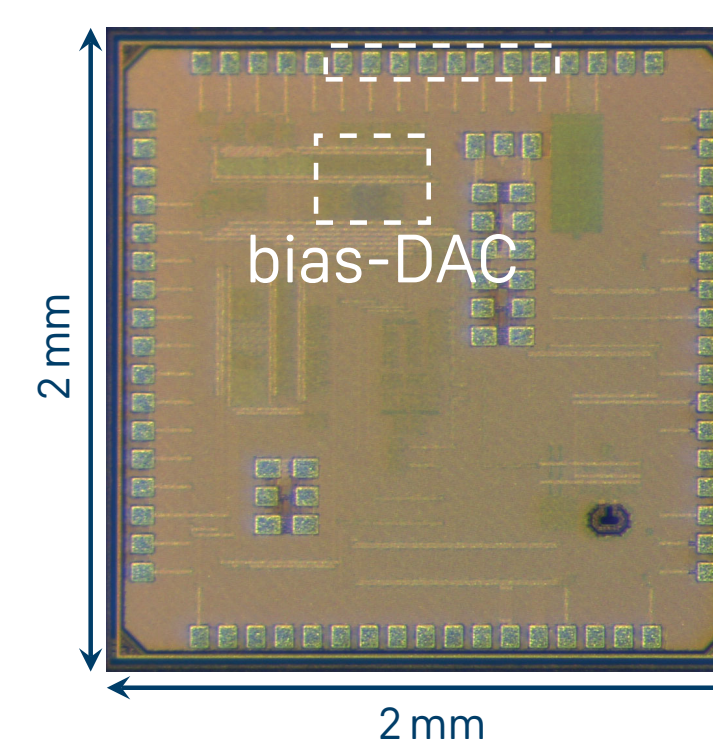


Fig.2: Die photograph of the IC with the bias-DAC and its outputs highlighted. The approximate DAC area is 0.14 mm².

Power consumption and recent leakage levels would allow for ~ 4 nW/ch at 10Hz refresh in this DAC architecture [7,8]

Qubit

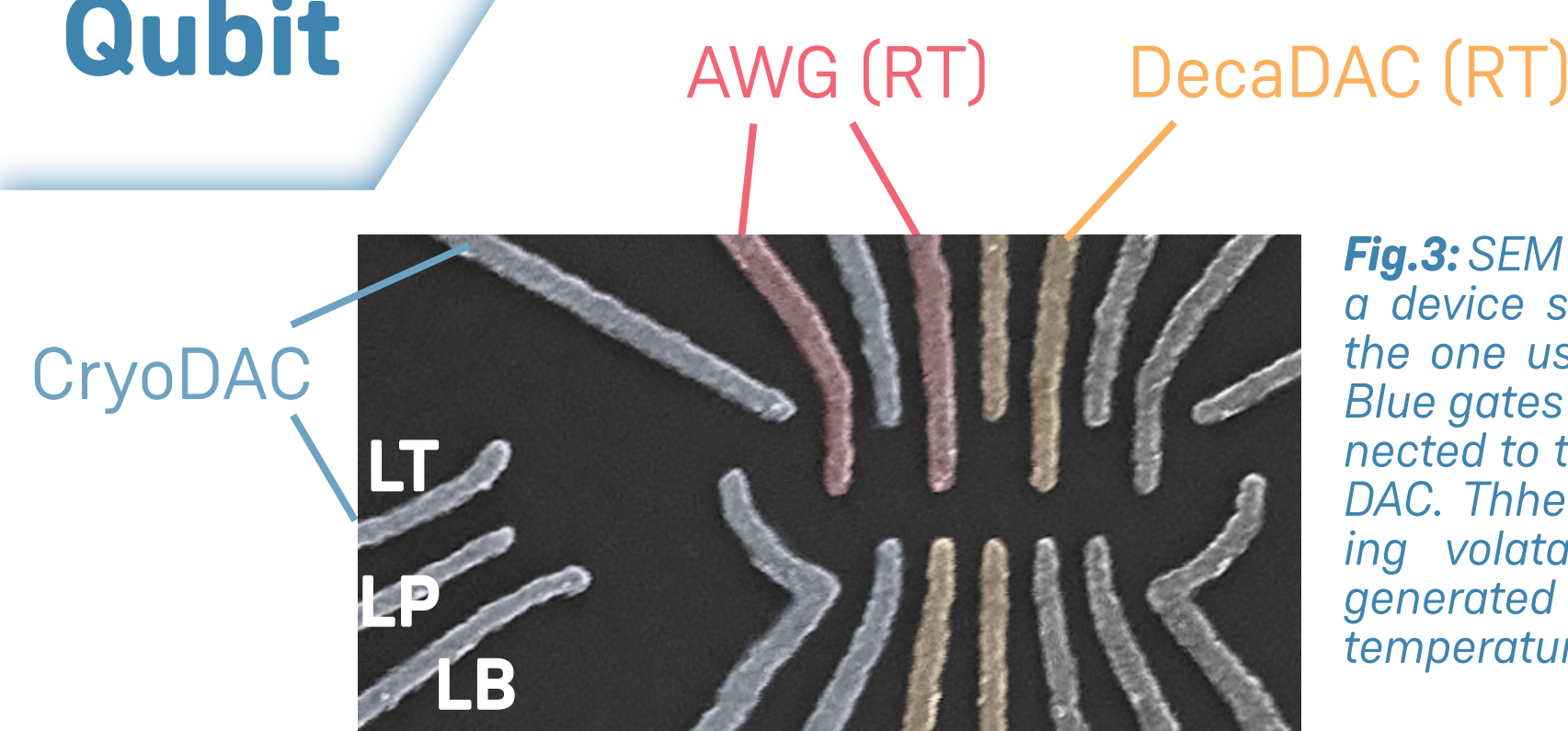


Fig.3: SEM Image of a device similar to the one used here. Blue gates are connected to the CryoDAC. The remaining voltages are generated at room temperature.

Run-of-the-mill GaAs Qubit Device

- High fabrication and tuning yield makes it ideal for proof of principle measurements
- Single Layer Ti/Au gates are fabricated on a doped Al-GaAs/GaAs heterostructure
- We shift 2DEG potential to 1 V to accommodate the CryoDAC output voltage range

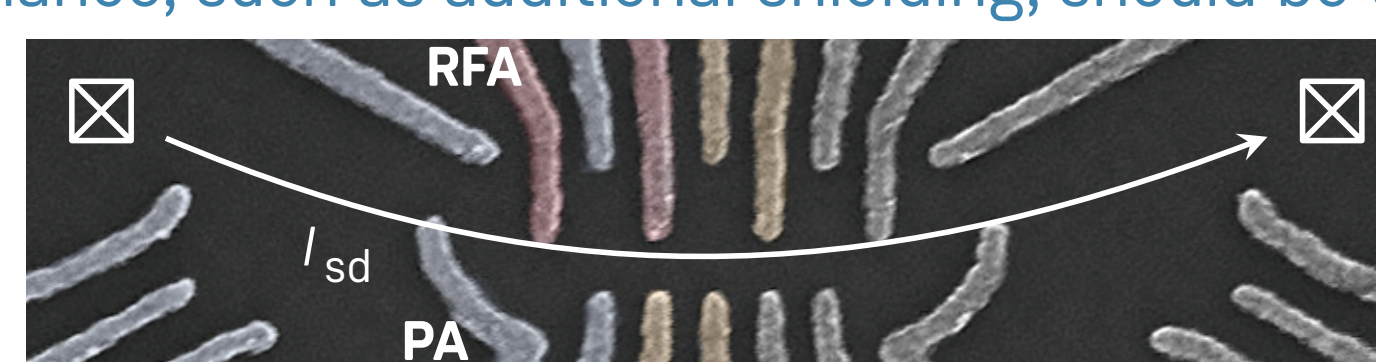
Voltage Stability

We benchmark the voltage stability by measuring transport across the GaAs device:

- Form QPC using one voltage from RT and one from the CryoDAC
- Signal average at the DACs nominal refresh rate

There are multiple interesting results:

- Large 100 μ V ripple when refreshing the QPC gate, possibly due to charge injection
- Eight ripples corresponding to the cyclic refresh of the DACs output channels
- Cross talk effects might be relevant, so steps to increase the analog performance, such as additional shielding, should be taken



SET

We form a sensing quantum dot using only voltages from the CryoDAC

- We can form a multi-electron dot in transport to measure the resulting electron temperature
- Coulomb oscillations are clearly visible
- We measure Coulomb diamonds to obtain lever arm

Measurements indicate an electron temperature of around $T_e \approx 550$ mK

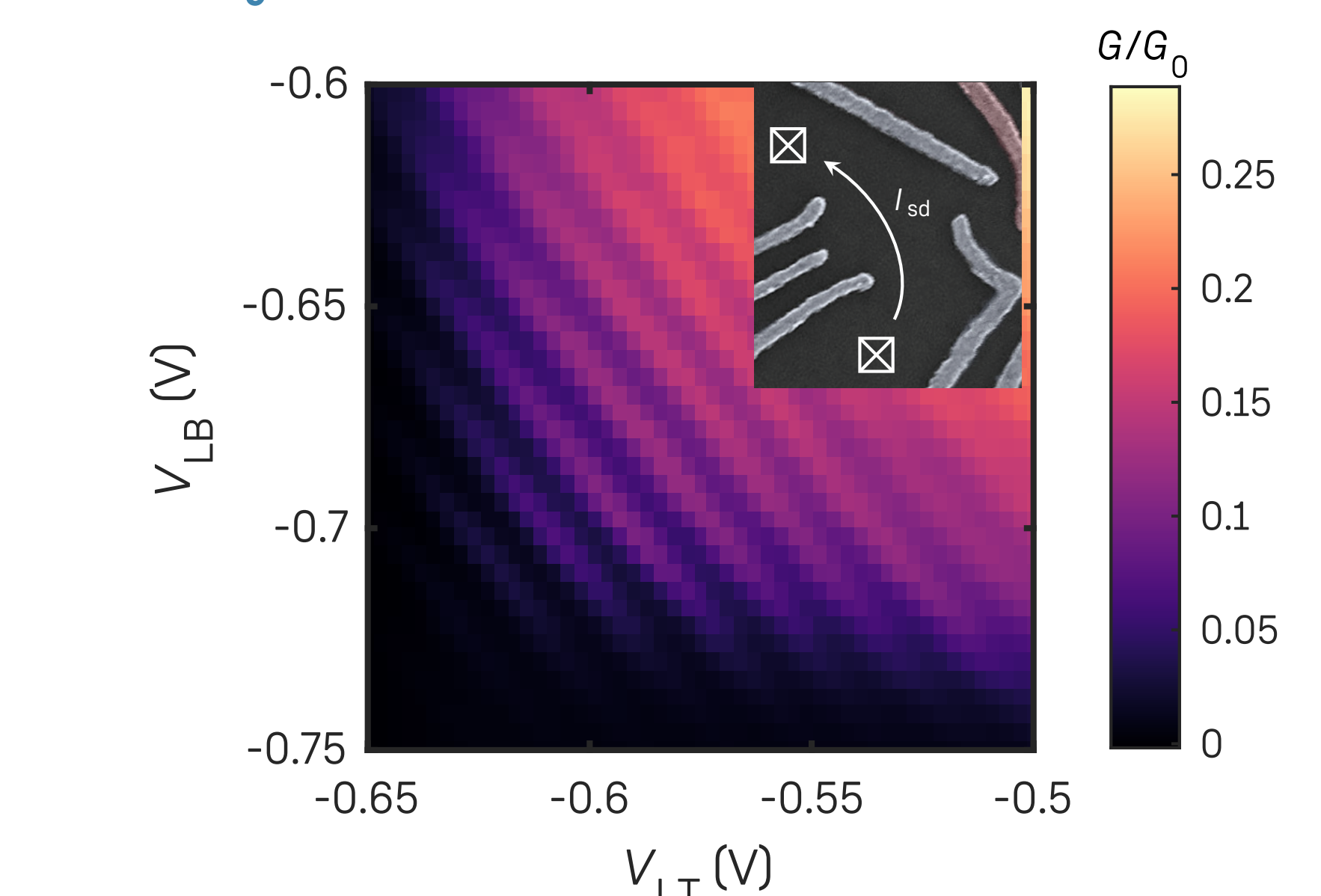


Fig.4: (top) Current path and measured conductance as a function of barrier gate voltages. Clear Coulomb oscillations are visible using only voltages generated below 1K.

(left) Conductance measurement at low bias of one of the lower peaks. Using previously measured Coulomb diamonds to extract the lever arm we can fit the width and obtain the electron temperature.

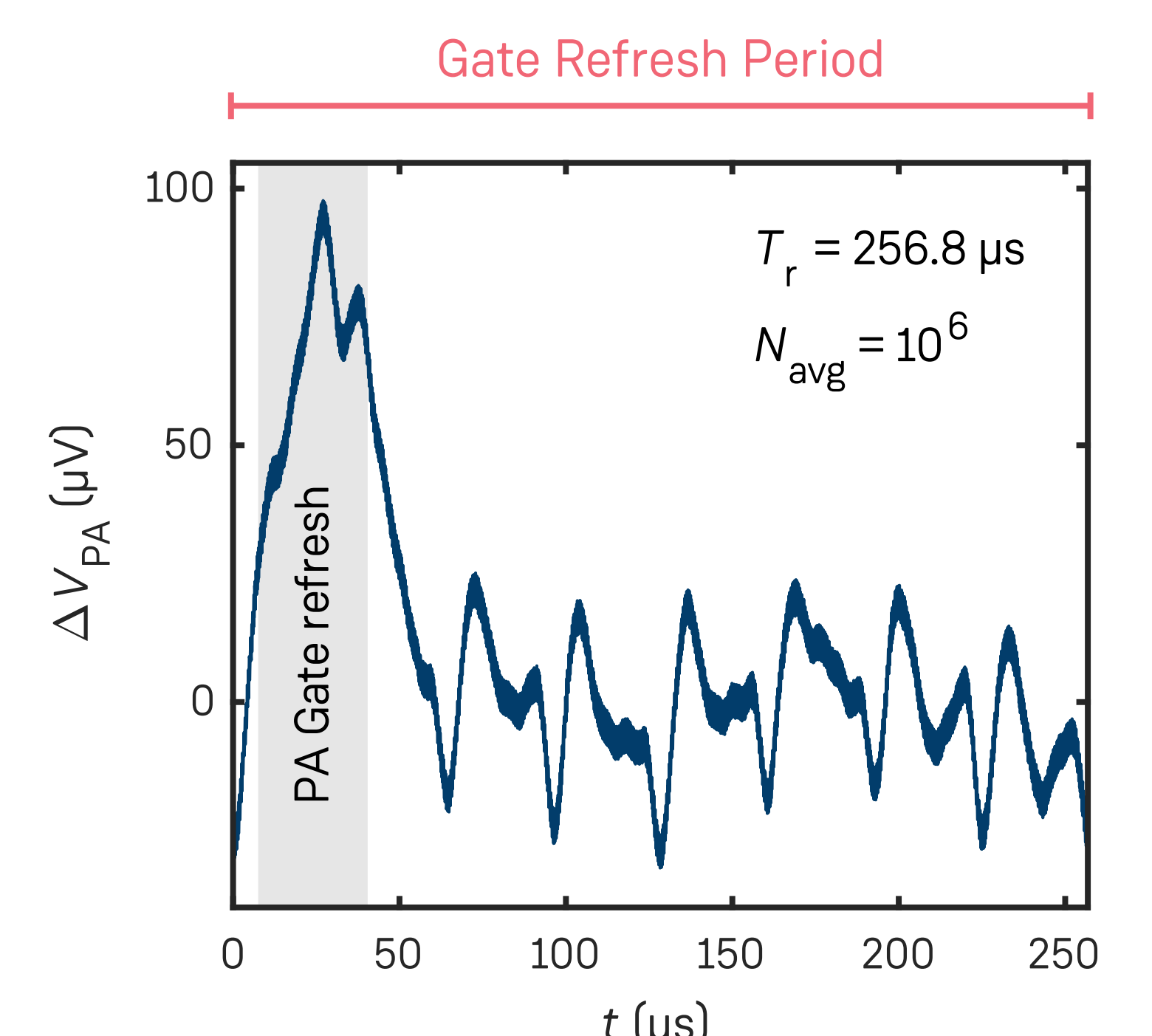


Fig.5: (left) Current path for the transport measurement. RFA and PA form a QPC. **(top)** Signal averaged gate voltage over a DAC refresh period.