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Terbium scandate thin films were deposited by e-gun evaporation on (100) silicon substrates. Rutherford backscattering spectrometry and x-ray diffraction studies revealed homogeneous chemical compositions of the films. A dielectric constant of 26 and *CV*-curves with small hystereses were measured as well as low leakage current densities of <1 nA/cm^2. Fully depleted *n*-type field-effect transistors on thin silicon-on-insulator substrates with terbium scandate gate dielectrics were fabricated with a gate-last process. The devices show inverse subthreshold slopes of 80 mV/dec and a carrier mobility for electrons of 225 cm^2/V·s was extracted. © *2010 American Institute of Physics*. [doi:10.1063/1.3275731]

The steady reduction of feature size in silicon-based integrated circuits over the past five decades recently required a replacement of silicon dioxide with a hafnium-based gate dielectric to reduce leakage currents and power dissipation. In order to continue scaling, higher-κ dielectrics with even larger dielectric constants ($\kappa > 20$) are now desired.[1,2] With respect to these demands the rare earth based oxides and among them the rare earth scandates (REScO$_3$—RE denoting a rare earth element) show very promising properties as amorphous gate dielectrics. They cover a wide range of dielectric constants κ from DyScO$_3$ and GdScO$_3$ with $\kappa = 22–23$ (Refs. 3 and 4) to LaScO$_3$ with $\kappa = 28$,[5] and even SmScO$_3$ with even $\kappa = 29$.[6] Both, bandgap and bandoffsets of these materials to silicon are sufficiently large.[7] Smooth, amorphous films can be deposited by different deposition techniques and most of the scandates remain amorphous in contact with silicon even when heated up to 1000 °C.[3,4] Moreover, the deposition of high quality GdScO$_3$ thin films with complementary metal-oxide semiconductor compatible atomic layer deposition has been demonstrated.[8,9]

Here, we report on the growth and characterization of amorphous terbium scandate (TbScO$_3$) thin films deposited by electron beam evaporation and their implementation as gate dielectrics in fully depleted silicon-on-insulator (SOI) transistors. A stoichiometric ceramic target made from a pressed and sintered mixture of the metal oxides was used as the evaporation source. RCA cleaned *p*-doped (100) silicon ($1–10$ Ω cm) was used as the substrate material. Prior to deposition the 2×2 cm^2 large substrates were etched in 1% hydrofluoric acid solution to remove the chemical oxide from the surface. The depositions were carried out in vacuum at a pressure of $(1–5) \times 10^{-6}$ mbar and at a deposition temperature of 600 °C. To improve the electrical properties of the films the samples were postdeposition annealed at 400 °C for 10 min in oxygen at atmospheric pressure. This postdeposition annealing leads to an additional growth of a silicate-like layer at the higher-κ/Si interface (determined by

x-ray photoelectron emission spectroscopy, not shown) and ensures low leakage current densities. It also limits, however, the lowest achievable capacitance equivalent thickness (CET) of the films.

The as-deposited films were found to be amorphous as revealed by x-ray diffractometry (XRD) as shown in Fig. 1 for a 19 nm thick film. In order to determine the kinetic stability of the amorphous phase to crystallization, this layer was annealed in a nitrogen ambient for 10 s at different temperatures and repeatedly measured with XRD. Those measurements are included into the graph in Fig. 1. Even at 1100 °C the film does not crystallize as seen by the absence of peaks in the XRD measurement, except for a small broad peak around 30° which is likely due to short-range order of the elements. The different noise level of the curves stems from different integration times.

The stoichiometry of the films was analyzed employing Rutherford backscattering spectrometry (RBS) with 1.4 MeV He$^+$ ions. A ratio of Sc:Tb$=0.89–0.95$:1 was determined revealing a slight scandium deficiency of the films (see Fig. 2). The electrical properties of the rare earth scandates have, however, proven to be rather insensitive toward stoichiometry variations as shown for dysprosium scandate.[10]
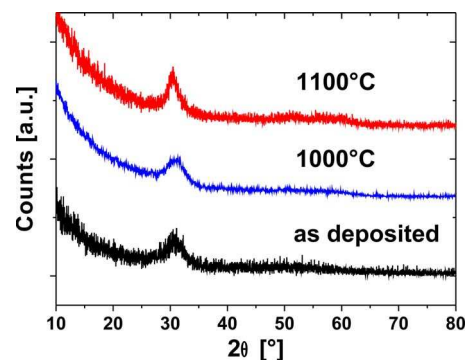

FIG. 1. (Color online) XRD measurements of a 19 nm thick TbScO$_3$ film before and after annealing at 1000 or 1100 °C, respectively. The absence of sharp peaks indicates an amorphous structure of the films.

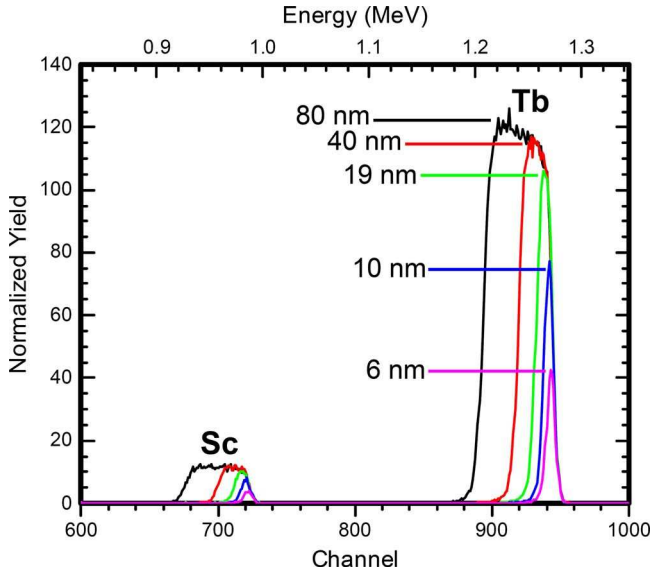a)Author to whom correspondence should be addressed. Electronic mail: j.schubert@fz-juelich.de.

FIG. 2. (Color online) RBS spectra of $TbScO_3$ thin films with thicknesses ranging from 6 to 80 nm.

FIG. 4. (Color online) CET plot of $TbScO_3$ thin films with varying thicknesses. From the slope of the linear fit a dielectric constant of $\sim$26 is determined. The inset shows an *I-V* curve of the 6 nm film.

For the electrical characterization of the films, metal-oxide-semiconductor (MOS) capacitor structures were prepared by dc sputtering of $\sim$100 nm TiN through a shadow mask for the top contacts. An ohmic backside contact was realized by e-gun deposition of $\sim$120 nm Al on the backside of the samples followed by a drive-in anneal at 400 °C for 10 min in a forming gas atmosphere (10% H_2/90% N_2). The electrical characterization of the capacitor structures was performed using an HP 4192A impedance analyzer for *C-V*-measurements and a Keithley 4200 SCS semiconductor characterization system for leakage current measurements.

Figure 3 shows *C-V* curves for a set of samples with different $TbScO_3$ thicknesses ranging from 6 to 80 nm. The thicknesses stem from x-ray reflectivity measurements. The hysterisises of the curves are negligible and, interestingly, only a slight positive flatband voltage shift depending on the film thickness is observed. The interface state densities derived from *C-V* as well as *G-V* (conductance-voltage) measurements using Terman's and conductance method[11] lie in the low to medium 10^{11}/eV cm^2 range.

From the capacitance value in accumulation, e.g., at -2 V, for each $TbScO_3$ film one can calculate a CET. The CET value corresponds to the thickness of a conventional silicon dioxide gate dielectric having the same electrical capacitance as the higher-κ film if quantum effects are neglected. CET plotted versus the physical layer thickness (Fig. 4) provides a dielectric constant of 26 and an interfacial SiO_2 thickness of $\sim$2 nm. The inset of Fig. 4 shows an *I-V* curve of the thinnest $TbScO_3$ sample with a physical thickness of 6 nm and a CET=2.7 nm. At $V_{FB}-1$ V the leakage current is below 1 nA/cm^2.

In order to investigate the influence of an alternative gate dielectric on the mobility of charge carriers in silicon, fully depleted long channel nMOS field-effect transistors (nMOSFETs) with $TbScO_3$ gate dielectric and TiN gate electrodes were prepared on SOI substrates with a silicon thickness of 25 nm in a gate last process described elsewhere.[12] In contrast to Ref. 12 the source/drain implantation dose (3×10^{15} cm^{-2}) as well as the activation temperature (1050 °C) were increased to achieve a lower source/drain resistance. For comparison purposes devices with a conventional 3.5 nm thick thermally grown silicon dioxide gate dielectric were prepared with the same process and subsequently characterized.

The transfer and output characteristics of a device with $TbScO_3$ gate dielectric and 20 μm gate width and 10 μm gate length are presented in Fig. 5. For both sets of curves pronounced linear and saturation regions can be distinguished. An inverse subthreshold slope of $\sim$80 mV/dec is reached. A process-related drain voltage-dependent leakage current in the transfer characteristic limiting the achievable I_{on}/I_{off} ratios is, however, visible whose origin is not clear as yet.

The electron mobility μ in the presence of the higher-κ dielectric was extracted from a linear fit of the $I_D/\sqrt{g_m}$ curve above the threshold voltage and then plotting the channel resistance $1/A(A=\mu\times C_{ox}\times W\times V_{ds}/L)$ versus L, the gate length (Fig. 6). With the linear fit the carrier mobility can be determined as $\mu=1/(m\times C_{ox}\times W\times V_{ds})$, where m is the slope of the fit, C_{ox} is the oxide capacitance density extracted from *C-V* measurements of test structures, W is the gate width, and V_{ds} is the drain voltage applied.[13]
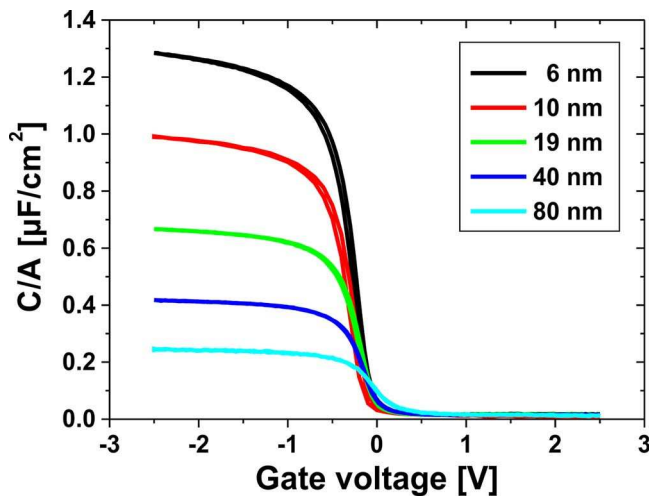

FIG. 3. (Color online) *C-V* curves of $TbScO_3$ thin films with thicknesses ranging from 6 to 80 nm. The hysteres and the flatband voltage shifts are negligible.
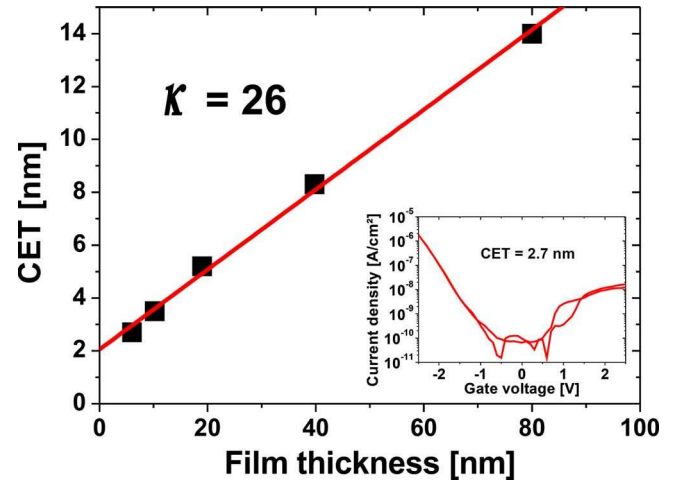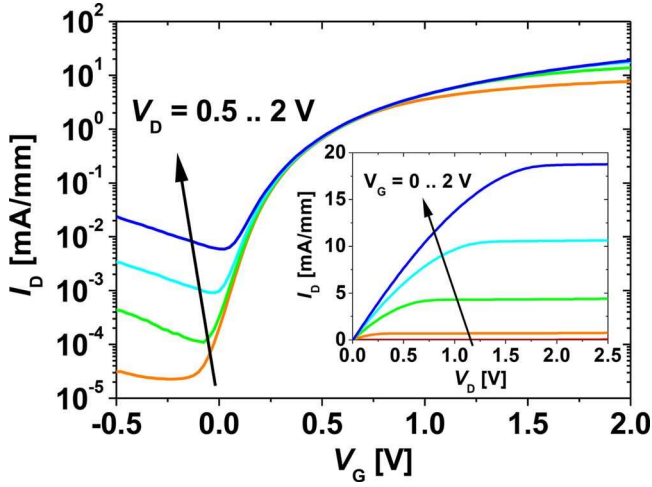
FIG. 5. (Color online) Transfer and output (inset) characteristics of an SOI transistor with a 5.5 nm thick TbScO$_3$ gate dielectric ($W=20$ μm, $L=10$ μm) and $V_D=0.5$, 1.0, 1.5, and 2.0 V.

Figure 6 compares the mobility plots of 1/A versus gate length for devices with conventional SiO$_2$ and TbScO$_3$ gate dielectrics and gate widths of 40 μm. In the conventional device electrons reach a mobility of 350 cm^2/V·s. For the alternative gate dielectric the value is reduced by 35% which
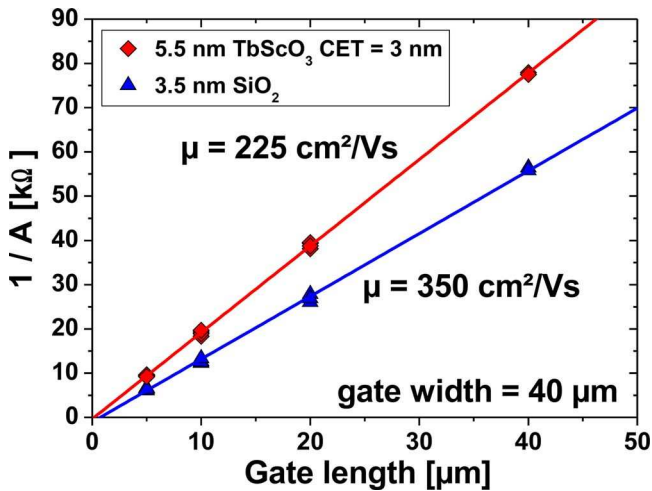

FIG. 6. (Color online) Plots of the channel resistance 1/A vs gate length for determination of the electron mobility in transistors with conventional SiO$_2$ and TbScO$_3$ gate dielectrics.

is comparable to the values reached with HfO$_2$.[14]

In summary, TbScO$_3$ thin films deposited with electron beam evaporation show promising properties for the use as a higher-κ dielectric. The films remain amorphous after 10 s annealing in N$_2$ atmosphere at 1100 °C. Electrical characterization of MOS capacitors with TiN top electrodes reveals nearly hysteresis free *C-V* curves. From a CET plot a dielectric constant of $\kappa=26$ is determined. The thinnest film with CET=2.7 nm shows a leakage current density of 1 nA/cm^2 at $V_{FB}-1$ V. With a gate last process, fully depleted nMOSFETs with a TbScO$_3$ gate dielectric have been prepared on thin SOI substrates. The output characteristics show pronounced linear and saturation regions of the drain current and an inverse subthreshold slope of 80 mV/dec are reached. Using the $I_d/\sqrt{g_m}$ method to determine the electron mobility in the devices resulted in a mobility of 225 cm^2/Vs which is about two thirds of those found for conventional SiO$_2$.

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